INRIA

INSTITUT NATIONAL DE RECHERCHE EN INFORMATIQUE ET EN AUTOMATIQUE

# *Team R2D2*

# *Reconfigurable and Retargetable Digital Devices*

*Rennes*

THEME COM

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# 1. Team

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# 2. Overall Objectives

## 2.1. Introduction

The problems tackled by the team R2D2 relate to the design of specialized systems on reconfigurable platforms. A hardware platform is a structure of Integrated Circuits (IC) containing a set of programmable components –general purpose or specific processor cores–, memories and generally specialized components.

Such a platform can be seen as an integrated architecture scheme, common to numerous algorithms belonging to a given application domain. This notion is the answer given by the designers of embedded systems to the increasing difficulty they have to implement their applications [43]. One can consequently imagine that in the future, most of the ICs necessary to the design of a complex system will be derived from a given existing platform. This design approach is an alternative to the IP-based (*Intellectual Property*) design approach, in which the system is built by the assembling of separately designed components. A reconfigurable platform includes a set of reconfigurable components (blocks of reconfigurable logic, reconfigurable data-path, flexible communication networks). In terms of area and power consumption, the reconfigurable resources enable a far more efficient use of the silicon than in programmable processors or in specialized components.

Future platforms will be highly parallel, heterogeneous, programmable and reconfigurable. Parallelism is the only way of reaching the performance level required by future applications. Heterogeneity results from the report that an efficient design is often composed of several subsystems, characterized by well-differentiated computation requirements. Programmability avoids freezing the functionalities. Finally, reconfigurability combines the speed of specialized solutions and the flexibility of traditional programmable components.

Our scientific objectives seek to profit from various methods (very high-level synthesis, behavioral synthesis, flexible compilation, floating-point to fixed-point conversion, etc.), contributing each one with its specificities, to the design of a part of a specialized system. The models and the underlying techniques allow the use of estimators, thus contributing to the choices of implementation, with a precise knowledge of the performance of the system, of its complexity and its power consumption.

## 2.2. Directions

Research undertaken within the team R2D2 aims at facilitating the design of reconfigurable hardware systems, by proposing models of architectures and associated design methodologies which favor the adequacy between the algorithms of the applications and the architectures supporting the implementation. The team links together three main directions.

### *2.2.1. New architectures and technologies*

Our studies, motivated by the constraints of high-performance, flexibility, and low-power consumption, focus on the following topics:

- the study of new organizations of reconfigurable structures offering the speed of specialized solutions and the flexibility of traditional programmable components with regards to application areas like mobile telecommunications ;
- the application of advanced mobile telecommunication techniques to the design of Network-on-Chip (NoC) ;
- the study of architectures for low-power sensor networks ;
- the study of Multiple-Valued Logic (MVL) circuits and architectures.

### *2.2.2. Synthesis and compilation for reconfigurable platforms*

The implementation of an application on a reconfigurable platform requires the setting up of a large set of techniques which contribute, by successive refinements, to the implementation choices of the various parts of the application on the components of the platform. Our studies focus on the following aspects: synthesis of dedicated hardware accelerators, processor modeling and flexible compilation, floating-point to fixed-point conversion.

### *2.2.3. Study of applications*

Our privileged field of applications is that of third and fourth-generation mobile telecommunications. Moreover other application domains are considered: cryptography, image indexing, speech processing. The work concern the prototyping of applications on reconfigurable and programmable platforms.

# 3. Scientific Foundations

## 3.1. Panorama

R2D2 research activities are based on work resulting from two scientific communities whose competences are complementary for the design of hardware systems: the first relates to the design methods and tools for specialized architecture design and the second concerns signal processing and dedicated circuit architectures. We start with an outline presenting the evolution of specialized architectures. We then give some bases of our research.

## 3.2. New architectures and technologies

**Keywords:** *Network-on-chip, SoC, grain of calculation, low-power consumption, multiple-valued logic, reconfigurable architecture, sensor network.*

By the end of the decade, IC technology should allow the integration of a billion transistors on a chip, instead of few tens of millions today as illustrated by the document published by the SIA[1] (*Semiconductors Industry Association*). The hardware systems of the future equipments will be miniaturized – one now usually speaks about System-on-Chip (SoC) – while mixing architectures which will be highly heterogeneous and will include dedicated hardware accelerators.

Even if electronic CAD tools and associated design methodologies progressed much during last years, the design of new ICs is therefore not easier today. On the contrary, the distance between the capacities offered by the technology and the potential of the current design tools – the famous *technology gap*, – was never as large. A rather fundamental change in the way of designing circuits is noticed.

This evolution of the technology has an impact on the architectures of ICs. With the years, a migration is noted: from ASIC towards SoC, and in an immediate future towards reconfigurable programmable platforms.

- ASIC were prevalent between 1980 and 1995, and from now on are only used as particular blocks in more complex heterogeneous systems.
- The first SoCs were designed around 1995. Thanks to the increasing density of chips, a complex SoC usually integrates one or more processor cores (general purpose processor or digital signal processor), memory blocks (RAM, ROM, flash memory, EPROM, etc.), as well as many different interfaces useful for the correct working of the system. They combine hardware and software components. Their design rests on the use of synthesis, place and route tools, and libraries of reusable components.
- In the near future, SoC will evolve to platforms, which are structures of integrated architectures, common to a set of algorithms or applications belonging to the same field of applications. The design tools and methodologies must thus make it possible to design a specialized architectures starting from this basic architecture [51]. The platforms will allow the needs for a broader spectrum of applications to be satisfied, at the price of a reduction of the variety of designed circuits.

Associating flexibility with high-performance and energy efficiency, is a critical issue for embedded applications. This is particularly true for mobile applications. These three constraints are taken into consideration in our architecture studies.

[1] http://www.itrs.net/ITRS/Files/2002Update/Home.pdf

### 3.2.1. New reconfigurable architectures

These last years saw the emergence of new reconfigurable architectures [40], which are an alternative to the traditional performance/flexibility compromise, conditioning the choice between purely hardware (ASIC) or purely software (programmable processor) solutions. For application domain like mobile telecommunications, three main constraints have to be combined: high-performance, low-power consumption and flexibility. Grain of computation, reconfiguration schemes, are open research topics.

As an example, the Pleiades [48] project is an architectural platform supporting several grains of calculations – logic operations are treated as effectively as the arithmetic operations, – designed in order to consume a minimum of energy whatever the level of required performance. However, this platform does not make it possible to support the set of constraints previously discussed because of the static feature of its reconfiguration which limits it to certain field of applications, the coding of words having been the support of the study.

In addition to these two examples, many reconfigurable architectures are based on FPGA-type circuits and the majority of them, such as GARP [41], NAPA [49], Chimaera [50], integrate a traditional programmable processor in charge of the sequencing of the treatments on the reconfigurable block. Other architectures such as Piperench [38] or RaPiD [33] can be reconfigured at a higher level, respectively at the operator and functional level. The concept of grain of calculation indeed constitutes an interesting and significant research subject. The majority of the FPGA circuits are *fine grain* since they can be reconfigured at the bit level, which contrasts with the way in which the programmable processors handle words (32-bit words for a number of them). When bit-level reconfiguration is not required by the application, coarse-grained structures must be built starting from the elementary blocks of the reconfigurable structure, which results in a over-cost of the circuit. To limit this over-cost, new coarse-grained reconfigurable architectures are proposed. It results in structures in which the elementary blocks correspond to arithmetic logic units, multipliers, memories, etc. In addition to Piperench and RaPiD already mentioned, the architectures Matrix [35] at MIT, MorphoSys [46] at the University of California at Irvine, can be quoted. And among the commercial realizations: the array of reconfigurable arithmetic logic units of Elixent [2], and the XPP processors of PACT[3].

### 3.2.2. Network on Chip design

The rapid growth of device densities on silicon has made it possible to deploy complete systems (SoC) using validated IP blocks. The increasing number of blocks needed to integrate all the functions required by a complex application shows the limitations of the current solution which consists in having a common interconnection resource (a bus). Among those limitations stand the increasing noise sensibility and the scalability of the interconnection scheme. In order to control precisely the electrical and scalability parameters [34] of the interconnect, in-chip communications have to be organized. A new paradigm is rising to face the interconnect issue [32]. The Network on Chip (NoC) concept proposes to use well-defined network layers to build the interconnection scheme. It separates the communication process into three different layers which provide the other layers with services (error detection or correction, routing or packetizing for example). A NoC is dedicated to the reliable and efficient routing of information grouped in packets (with redundancy information, routing information, etc.).

Assuming that the voltage swing on wires will decrease in the next few years, the reliability of the physical layer will decrease. The challenge is to provide a reliable, efficient and low-power link to meet the requirements of future SoC.

### 3.2.3. Wireless sensor networks

Wireless sensor networks are groups of sensors interconnected with each other through wireless links. The aim of these sensor networks is to collect information from the area and to relay it through the network. Since several years, research in telecommunication, wireless networks, and signal processing has focused on this topic that raises new challenges in wireless communication [55]. First, the autonomy or the lifetime of a sensor network must be very high, since the sensors can be integrated in concrete, in the soil or even in

[2] http://www.elixent.com/
[3] http://www.pactcorp.com/

the body of living beings where the replacing of the batteries is impossible or difficult. Energy-scavenging techniques can be used for that purpose. Then, these networks have to be ad-hoc, so that they can self-organize and cope with local sensor breakdowns, for example when some sensors run out of power. Another important singularity is the fact that the data rate needed by the applications should be quite low, since the data does not have to be send continuously, but only when changes occur. Many applications have been proposed, in miscellaneous domains of activity. In agriculture, building, bridges, transport, military applications, enemy monitoring, chemical and bacteriological monitoring, emergency after earthquakes. Many wireless systems already exist and are commercially successful. Their specifications have generally been developed in order to maximize the spectral efficiency. In sensor networks, the energy is more critical than the available spectrum. For these kind of applications we should rather maximize the power efficiency than the spectral efficiency. A communication system can be described functionally by dividing the processing in layers. The OSI (Open Systems Interconnection) model describes seven layers for the processing. The problem is that the design of a communication system cannot efficiently be done each layer separately because they are coupled to each other. It is not enough to make optimizations on each layer separately. That is why designing a power-efficient system must take into account this coupling, by making cross-layer optimizations [37]. For that reason, it is better to consider few layers. We worked with a fragmentation of the protocol stack in only two layers. The higher-level part includes the aims of OSI application, presentation, session, transport, and network levels. The lower-level part includes the aims of OSI data-link and physical levels. The lower-level part considers a transmission between two neighbor nodes and has to optimize the communication from this point of view. The higher-level part considers a transmission between generally distant applications, assuming that the lower-level communication used are energy-efficient. This fragmentation has already been used in [53], and can be justified by saying that networking issues are coupled together only in the higher-layer part, while the channel management issues are coupled only in the lower-layer part.

### *3.2.4. Multiple-Valued Logic architectures and circuits*

Nowadays, numerical systems are exclusively based on a binary representation of numbers and computations. It was shown that the use of a higher number of logical states can reduce the number of interconnection wires and the memory area [36]. It also optimizes the arithmetic processing.

ICs performances are limited by complex wiring –a great amount of the chip performance is devoted to interconnection–, large propagation delay and high-power consumption. Using Multiple-Valued Logic (MVL) techniques, the amount of interconnections and the power consumption caused by important switching activity on each node of a circuit can be reduced. The SUpplementary Symmetrical LOgic Circuit structure (SUSLOC) is a new promising approach for the implementation of MVL functions in voltage-mode. It combines low-energy consumption and a speed equivalent to binary CMOS structures.

## 3.3. Synthesis and compilation for reconfigurable platforms

**Keywords:** *ASIP*, *IC*, *architecture description language*, *data coding*, *design methodology*, *fixed-point arithmetic*, *flexible compilation*, *high-level synthesis*, *parallel architecture*, *precision*, *retargetable compilation*, *specialized processor*.

### *3.3.1. Dedicated hardware accelerator synthesis*

Although the architecture of ICs evolves to increasingly programmable and reconfigurable solutions, it remains that the future silicon systems will continue to integrate specialized hardware components. The design of such components rests on the use of synthesis techniques.

Today circuits synthesis starts from high-level specifications. The specification of programs carrying out regular computations in the form of recurrence equations allows powerful static analyses and transformations of programs for the derivation of regular architectures [4].

The base of our research is the polyhedral model, which is well-suited to the expression of the calculation parts applications and which allows the expression and the handling of systems of recurrence equations.

There exist many academic environments prototypes for the automatic synthesis of specialized architectures starting from high-level specification: for example, Diastol, Presage, Hifi, Cathedral, Sade, PEI and MMAlpha. Tools performing a high-level synthesis from the C language now exist on the market: tools based on SystemC[4] like *CoCentric SystemC Compiler*[5] of Synopsys, *A|RT Builder* of Adelante Technologies/Frontier Design, tools based on C and its extensions as *Celoxica DK1 Design Suite* [6] of Celoxica.

Few tools rest on a true parallelization but many research projects explore this approach: Flex[7] and Raw[8] at MIT, Piperench[9] at Carnegie-Mellon, Garp[10] at Berkeley, Pico [52] at HPLabs Palo Alto, Compaan[11] in Leiden.

Alpha [6] and MMAlpha, developed in the project-team Cosi, evolved from Diastol and constitute today a practical environment for the handling of recurrence equations and the high-level synthesis of dedicated hardware accelerators. The work is done in close cooperation with the team CompSys (LIP, ENS Lyon).

### 3.3.2. Processor modeling and flexible compilation

Hardware description languages like VHDL or Verilog are largely used to model and simulate processors, but mainly with the aim to design hardware. The design of SoC requires methodologies and tools for the exploration of the architecture design space. This exploration passes by the use of architecture description languages (ADL), adapted to the specification of the SoC architecture models. Very early in the design process, they play a role on the one hand for the validation of SoC architectures, and on the other hand for the automatic generation of the software development tools necessary to the software and hardware design of the architecture.

Most of the existing architecture description languages aim at the specification of processor architecture, by privileging either the synthesis, or the generation of compilers, or the generation of simulators, but very seldom the whole. None of the existing languages is really directed towards architectural exploration.

In the category of architecture description languages mainly directed towards processor hardware synthesis, one can quote Mimola, developed at the university of Dortmund, and used to describe target machines in the MSSQ and Record [45] compilers. Mimola is very close to hardware description languages like VHDL or Verilog. A Mimola description can be employed for the synthesis, simulation, and code generation, after extraction of the instruction set.

With regard to the architecture description languages mainly directed towards compilation, one can quote nML, designed at the university of Berlin, ISDL proposed by the MIT, MDES developed at the university of Illinois, Expression developed at the University of California at Irvine.

With regard to the architecture description languages mainly directed towards simulation, one can quote LISA [47], developed at the university of Aachen. LISA allows the generation of cycle-accurate simulators for DSP processors. Both the structure and the behavior can be modeled.

The existing architecture description languages can be classified according to the modeling level: behavioral or structural. A language like Mimola is of structural level, languages like nML and ISDL are of behavioral level. LISA, Expression and MDES mixes the two levels of modeling.

There is no standard as regards architecture description languages. The ARMOR language developed in the project-team Cosi, constitute a practical approach for the modeling of complex architectures. It is suited to architectural exploration and automatic generation of software development tools (compiler, simulator, processor design tools, etc.). .

### 3.3.3. Floating-point to fixed-point conversion

The efficient implementation of an algorithm on a specialized processor, such as for example a DSP (Digital Signal Processor) or an ASIP (Application Specific Instruction-set Processor), or on a hardware structure, such

[4] http://www.systemc.org
[5] http://www.synopsys.com/products/cocentric_studio/
[6] http://www.celoxica.com/products/tools/dk.asp
[7] http://flex-compiler.lcs.mit.edu
[8] http://cag.lcs.mit.edu/raw
[9] http://www.ece.cmu.edu/research/piperench/
[10] http://brass.cs.berkeley.edu/garp.html
[11] http://www.liacs.nl/~cserc/compaan/index.html

as an ASIC or a FPGA (Field Programmable Gate Array), requires for reasons related to cost, consumption or silicon area constraints, the use of fixed-point arithmetic, whereas the algorithms are usually specified in floating-point arithmetic. This conversion is a tiresome task and error-prone if it is carried out manually. Indeed, some experiments [39] showed that the time devoted to this conversion step is relatively significant, manual conversion being able to represent up to 30% of the total time necessary to the implementation of the algorithm. Let us note in addition that the time-to-market constraint requires the use of high-level development tools, allowing to automate certain tasks.

The existing methodologies for fixed-point data automatic coding [44][54] carry out a transformation from floating-point data representation into a fixed-point representation, without taking into account the architecture of the target processor. However the analysis of the influence of the architecture on the precision of computation and the various phases of the code generation shows the need for taking the architecture features into account and for coupling the coding and code generation processes to obtain an implementation of quality in terms of precision of calculations and execution time.

Data coding optimization must be carried out under precision constraint, and it is thus necessary to determine the signal-to-quantization noise ratio (SQNR) of the application. The SQNR determination methods [42] are generally based on simulation. But within the framework of the data coding optimization these methods use an iterative process leading to high times of optimization. The study of analytical techniques offers new perspectives for the accuracy evaluation.

# 4. Application Domains

## 4.1. Panorama

The privileged field of applications is that of third- and fourth-generation mobile telecommunications.

According to the cooperations, other application domains are therefore considered: image indexing, cryptography, and speech processing.

## 4.2. Mobile telecommunications

The future generations of telecommunications constitute a privileged field of applications for IC designers because of the diversity of the constraints to satisfy. In addition to the very high-level of performance – superior to 12 billion operations per second – resulting from the association of multimedia capacities and access techniques such as the WCDMA which these systems will have to support (known as 3G), is added the need for supporting the whole of the algorithms integrated into the standards of present generations (GSM, DEC, IS-95) and their evolutions.

From the point of view of hardware architectures, the next generation systems will have successively to deal with very different applications. Indeed, the common tasks in a third-generation communication chain handle variable data sizes according to *distance* separating the task from the transmitter or the receiver, – the application tasks handle data of high-granularity such as images whereas the tasks giving access to the transmission operate on bit-level data. Because of the importance of the application spectrum integrated into the future telecommunication standards, the treatments to be applied to these data will also be very diversified, which will result in very different calculation patterns. Even if each one of these constraints can be supported, the problem is much more delicate when they are combined, the time-to-market constraints impose the definition of development tools as portable as effective. In case of energy-aware products – lower than 500mW in peak, – this problem is insolvable if one limits oneself to the current architectural solutions.

# 5. Software

## 5.1. Panorama

**Keywords:** *library*, *polyhedral computation*.

Research undertaken by R2D2 is in the context of software and hardware tools for the design of hardware systems. In order to promote the studied techniques, several software prototypes are developed (Polylib, MMAlpha, BSS, ARMOR/CALIFE). Among those, three distributed software are presented: Polylib an *open source* library of calculation on polyhedron, MMAlpha for the high-level synthesis and BSS a platform for the design of circuits.

## 5.2. PolyLib

**Keywords:** *ASIC, CAD, architecture synthesis, data parallelism, functional programming, polyhedral computation.*

**Participants:** Patrice Quinton [contact], Tanguy Risset [CompSys, INRIA Rhône-Alpes].

The polyhedral Polylib library, developed in C, is an *open source* library of calculation on convex polyhedron. It was developed initially by Hervé Le Verge and Doran Wilde at INRIA Rennes. It is today maintained and developed with the LIP (ENS Lyon) and the ICPS of the university of Strasbourg. The handling of the domains used in the recurrence equations or spaces of indices described by nested loops justifies the use of such a library. This library is currently used (independently of MMAlpha) by several research organizations (in England, the United States, the Netherlands, and in France).

To know some more, refer to *http://www.irisa.fr/polylib* or contact Patrice Quinton.

## 5.3. MMAlpha

**Keywords:** *ASIC, CAD, architecture synthesis, data parallelism, functional programming.*

**Participants:** Patrice Quinton [contact], Tanguy Risset [CompSys, INRIA Rhône-Alpes].

MMAlpha is a software which implements transformations on the Alpha language. The Alpha language was proposed by Christophe Mauras during his thesis in 1989. The implementation is carried out in the Mathematica language (from where the name MMAlpha) and is built on the Polylib library.

Alpha program transformations are implemented by combining the Mathematica language and the Polylib library. The principle is to derive either an architecture, a sequential or a parallel code starting from an algorithmic specification of a problem. These transformations are semi-automatic, i.e. the actions to be performed are indicated by the user but the transformation itself is carried out by MMAlpha. Automatic transformations are also available, and provide in some cases satisfactory results.

The design methodology is inherited from the method of systolic array synthesis. This field is studied from the theoretical point of view, and results of these research are implemented and experimented in the MMAlpha software. This software makes it possible to test various existing synthesis strategies, to study various possibilities of parallelization and to generate an architectural description of a circuit thanks to the AlpHard format (subset of the Alpha language). The interface between MMAlpha and logic synthesis tools is done thanks to a translation towards VHDL.

The software was the implementation support of many theses carried out at Irisa. It is used by several research teams within the framework of collaborations with R2D2. It is one of the only tools making it possible to describe an algorithm and its hardware implementation in the same language and to deduce this implementation with proven transformations.

To know some more, refer to *http://www.irisa.fr/R2D2/ALPHA/* or contact Patrice Quinton.

## 5.4. BSS, BOOST

**Keywords:** *architecture synthesis, circuit design, low-power consumption, placement.*

**Participants:** Daniel Chillet [contact], Sébastien Pillement, Olivier Sentieys.

The BSS (*Breizh Synthesis System*) software platform for circuit design proposes a set of tools for the capture of application description (in VHDL or in C), the compilation, the simulation and the synthesis of architecture. This one is developed in order to make the tools accessible by Internet.

The platform is currently composed of the following modules.

- A set of programs (C and VHDL compilers, selection, scheduling, code generation) allowing the synthesis of circuits.
- Graphic interfaces, *PUDesigner and GFDesigner*, allowing the visualization and the handling of the data flow graphs and architectures.
- A tool for power estimation at the architectural level, *PowerCheck*, operating from the architectures generated by the synthesis. It also uses as an input a file of parameters which makes it possible to characterize the technology of the circuit and the physical capacities of the chips. The signal can be specified in two different ways: either by its probabilities according to a model (white noise, DBT), or in the form of a file of vectors from which are extracted the probabilistic characteristics. As output, PowerCheck provides a report indicating the average powers dissipated by each part of the control and processing units. PowerCheck also gives the dissipated powers cycle by cycle by the various modules.
- A tool for area and delay interconnection estimation, *Jfloorplanner*, operating at the architectural level. The input of the tool consists of a *netlist* generated by BSS. This netlist contains the whole of information related to the components and their interconnections. The tool provides indications concerning the final area of the floorplan, the length of the interconnections as well as the interconnection delays related to these lengths. A display of the estimated floorplan is available and can be used in order to carry out quickly the place and route step with standard CAO tools.

BOOST (Breizh Object Oriented Synthesis Tools) is an evolution of the BSS platform which main objective is to facilitate the integration of new modules in the synthesis flow.

A global XML application defines the module list and the installation location. For each module, an XML application defines how the module has to be described to be included in the Boost platform. Several simple synthesis steps have been included in Boost. This platform was used as a demonstrator for the OSGAR project during the RNTL days in October (4-5 October in Rennes). Boost is developed in Java language and can be installed on solaris, windows or linux platforms.

To know some more, contact Daniel Chillet.

# 6. New Results

## 6.1. New architectures and technologies

**Keywords:** *CDMA, MVL, Network-on-Chip, NoC, SoC, System-on-Chip, grain of calculation, low-power consumption, multiple-valued logic, reconfigurable architecture, sensor network.*

Our studies, motivated by the constraints of high-performance, flexibility, and low-power consumption, focus on the following aspects:

- the study of new organization of reconfigurable structures,
- the memory hierarchy in specialized SoC,
- the use of advanced mobile telecommunication techniques applied to NoC design,
- the study of innovative architectures for low-power sensor networks,
- the design of multiple-valued logic circuits.

### 6.1.1. DART reconfigurable architecture

**Participants:** Sébastien Pillement, Olivier Sentieys.

The definition of the DART architecture led to the Ph.D. thesis of Raphael David in 2003 [3]. In order to validate the theoretical aspects and simulated performances of this new computation paradigm through a silicon prototype, a collaboration has started with the LIST laboratory of CEA. The aim of this joint research project is to integrate a DART cluster implementing the channel estimation in the 802.11a Wireless LAN norm. The algorithmic complexity of channel estimation is 1784 MOPS and 356 MDPS (million of division per second). A VHDL model of DART at the register-transfer level has been designed. It is compatible with the SystemC cycle-true bit-true simulator. The synthesis of a DART cluster including six reconfigurable datapath and two dedicated dividers on a 130 nm CMOS technology from STMicroelectronics, leads to a 200 MHz clock frequency (i.e. 4800 32-bit MOPS plus 400 MDPS) for less than 10 square millimeters.

Other studies, such as the coupling of a DART cluster with other resources on a SoC, are pursued. A first model of coupling with a general purpose microprocessor is proposed in [16]. This demonstrates the potential of reconfigurable accelerators in order to increase calculation power and flexibility of a SoC. This work is done through a collaboration with ENIS (*École Nationale d'Ingénieur de Tunis*, F. Ben Abdallah Ph.D.).

### 6.1.2. Memory hierarchy in specialized SoC

**Participants:** Daniel Chillet, Olivier Sentieys.

Our research aims at defining a global memory organization model suited to SoC and a methodology which allows the designer to explore different memory organization solutions.

SoC architectures already propose large on-chip memory, with several memory banks and memory hierarchical levels (e.g. cache memory). In these systems, the main problem concerns the memory exploration in relation with the application needs. Several problems could be addressed in this context, such as cache, scratch-pad, and multi-bank memory. We focus our research on designing methodologies for optimal memory hierarchies. A first model has been defined for dedicated SoC and for large reconfigurable architecture such as FPGA circuits. This work is done through a collaboration with the *École Nationale Polytechnique d'Alger* (L. Abdelouel Ph.D.).

### 6.1.3. Reconfigurable architecture for control intensive applications

**Participants:** Stéphane Chevobbe, Olivier Sentieys.

Previous works have shown that reconfigurable architectures are particularly well-adapted for implementing regular processing applications. Nevertheless, they are inefficient for designing complex control systems. We work on a new concept of reconfigurable dedicated to the control architecture which can manage instruction parallelism as well as task parallelism. As the parallelism of an application can be well described by Petri nets, the architecture is able to directly implement Petri net on its structure. The core of the architecture is a network of asynchronous automatons. As the number of cells is limited, the concept of dynamic reconfiguration has been introduced to virtually grow the size of the architecture. Furthermore, the architecture is auto-adaptative, so it manages itself the reconfigurations according to the geometry of the application graph. After the definition of the paradigm of the RAMPASS architecture, our work consisted in evaluating the gain (performance, flexibility, power) of such an architecture. We realized two models of the architecture, one in SystemC to simulate the behavior of the architecture, and another one in RTL VHDL to estimate the performance and the area of the architecture.

### 6.1.4. NoC design using advanced mobile telecommunication techniques

**Participants:** Jean-Marc Philippe, Sébastien Pillement, Olivier Sentieys.

The increasing need of a low-power and high-speed interconnect lead us to investigate new signaling concepts. Among them stands the PAM (Pulse Amplitude Modulation) technique which consists in having multiple voltage levels encoded on a single wire. We have designed a quaternary link using custom transistors to overcome some of the interconnect problems. The foundry process is modified to meet the voltage threshold

requirements of our transistors. The quaternary link is composed of a binary-to-quaternary encoder and a quaternary-to-binary decoder. The encoder converts two binary signals into a quaternary one and the decoder converts back the quaternary signal into two binary ones.

The SPICE simulations of the circuit show a great improvement in terms of energy consumption for global interconnects. This is due to the reduction of the voltage swing of some transitions. The energy consumption reduction is about 50% with a 10mm wire and our system consumes less energy even for a 1mm wire (compared to a full-swing binary system). Another advantage of this approach is that the transistor count for the whole system is very low and represents 22 transistors (10 for the encoder and 12 for the decoder). This link also reduces by two the number of wires needed to transmit the information. This enables us to increase the inter-wire distance to reduce the crosstalk noise. This contributes to the reduction of the interconnect area.

We have proposed an analytical energy consumption model for quaternary links. This model enables to predict the dynamic energy consumption of a complete link as a function of the wire length, electrical and technological parameters and statistic distribution of the binary inputs.

### *6.1.5. Wireless sensor networks*

**Participants:** Mickaël Cartron, Olivier Sentieys.

The aim of our research is to optimize the energy efficiency of a wireless sensor network at the architectural and algorithm levels. We modeled the behavior of a low-level communication system, from the physical level to the packet retransmission system. The target of the processing is a dedicated architecture (ASIC), because of its lower power consumption compared to microprocessors or FPGAs. We modeled the bit-error-rate performance of the communication system and its power consumption as a function of several parameters (noise power, distance, packet size, amplification level). From analytical expressions of the performance and power separately, we can deduce the value of the power with a constraint of performance, which can be expressed as the energy consumed per successfully transmitted useful bit. With the help of this expression, we have highlighted an optimal operating point as a function of the input parameters. Recent results have shown that the use of this configuration for the architecture and for the communication system parameters allows to save up to 75% of the power, compared to the worst case technique.

### *6.1.6. Multiple-Valued Logic architectures and circuits*

**Participants:** Daniel Chillet, Ekue Kinvi-Boh, Olivier Sentieys.

The design of MVL functions rests on the SUpplementary Symmetrical LOgic Circuit structure (SUS-LOC). A library of basic MVL logic, memory and arithmetic cells has been designed, characterized and compared with classical binary CMOS implementations.

We described VHDL models of ternary basic logic and arithmetic cells and of some arithmetic processing units (adder, multiplier, shifter). These models take into account the variation of the power consumption and the delay according to the cell output capacitive load and they are used as components when describing the structural architecture of a ternary DSP core.

A collaboration with the SOI group at the Catholic University of Louvain-La-Neuve (UCL) has allowed to implement ternary functions in a $2\mu$ SOI CMOS process using the SUS-LOC concepts, with a first aim to validate our experimental estimations. A 64-tert SRAM and a 4-tert adder have been designed and fabricated at UCL. These two circuits represent the very first full-ternary circuit ever fabricated. They have been successfully tested using specifically fabricated test equipments.

## 6.2. Synthesis and compilation for reconfigurable platforms

**Keywords:** *architecture modeling ASIP design, architecture synthesis, communication, fixed-point arithmetic, flexible compilation, reconfigurable system, scheduler, synthesis, system on-chip.*

The implementation of an application on a reconfigurable platform, combining programmable processor cores and reconfigurable blocks, requires the setting up of a set of various techniques (architecture synthesis, flexible compilation, fixed-point code generation, profiling, etc.). They contribute, by successive refinements,

to the choices of implementation of the various parts of the application on the components of the platform. The research activities which we carry out aim at setting up methodologies allowing the implementation of various parts of an application on the various components of a platform. Current works concern the following aspects:

- the modeling of data-flow architectures using Alpha ;
- the automatic synthesis of optimized reconfigurable systems ;
- the synthesis of specialized microcontroller on FPGA ;
- the floating-point to fixed-point conversion ;
- the evaluation of fixed-point accuracy for non-linear systems ;
- the modelling of programmable processor cores ;
- the system modelling for dynamically reconfigurable architectures.

### 6.2.1. Modeling data-flow architectures using Alpha

**Participants:** Madeleine Nyamsi, Patrice Quinton, François Charot, Charles Wagner.

Our research aims at developing methods and tools to synthesize parallel architectures for data-intensive applications expressed using the Alpha applicative language. These methods are implemented in the MMAlpha software.

The Alpha language allows systems to be modeled using structured descriptions: some components can be separately represented, and later instantiated as an elementary block in a larger application. In many applications, these blocks have different clock rates, and it is the case for example, in the WCDMA (Wireless Code Division Multiple Access) air interface. We have been able to represent in Alpha multi-rate systems, by adding special components that model up- and down-samplers, and we have extended the structured scheduler of MMAlpha in order to find out the rates of all elementary blocks as well as the detailed schedule of each block. This research has been presented in [21].

### 6.2.2. Automatic synthesis of optimized reconfigurable systems

**Participant:** Christophe Wolinski.

Our aim is to investigate the communication synchronization problem inside the *Fabric* [12] reconfigurable architecture[12]. It was shown in [22] that the dynamic communication synchronization needs a lot of hardware resources for implementation and it has a high impact on the performance of the entire system. It was proven that the best solution can be obtained in the case of static scheduling. We have developed a novel method to obtain an optimized static schedule of CSP-like communications between a collection of concurrent hardware processes implemented on *System on a Programmable Chip* (SoPC) [31][30]. The hardware processes are the applications tailored *cells* in the Processor-Coupled Polymorphous Fabric implemented on the Altera Excalibur platform. The scheduling problem is defined and solved using a constraints programming approach [5]. This approach makes it possible to obtain optimal communication schedules in a number of real cases. It also makes possible to easily generate pipelined schedules that significantly improve the performance of the final implementation.

### 6.2.3. Specialized Microcontroller synthesis on FPGA

**Participants:** Ludovic L'Hours, François Charot.

This research aims at developing techniques to synthesize specialized microcontrollers on FPGA. The targeted applications are described in a high-level language such as C, where control strongly prevails (peripheral control driver, packet processing, etc). The main goal is to get small-sized circuits, with reasonable performances. The traditional approaches of architecture synthesis generally aim at maximizing the performance by

[12] This work is an extension of research on an automatic optimized reconfigurable system synthesis undertaken at Los Alamos National Laboratory, USA.

analyzing and paralleling the data flow, there are not suited to applications with complex control flow. Their intrinsic sequential feature naturally leads to use software compilation techniques.

A microcontroller synthesis technique based on the extraction of a specialized instruction set, starting from a given application is studied. The design of this instruction set is mainly leaded by application profiling information, but also by different estimators such as silicon area, cycle time. The microcontroller is then derived from this instruction set: the targeted architecture is currently a microcoded processor, but other kind of architectures such as RISC or VLIW could be considered.

### *6.2.4. Floating-point to fixed-point conversion methodology*

**Participants:** Daniel Menard, Nicolas Hervé, Daniel Chillet, Olivier Sentieys.

In our previous work, a methodology for the implementation of floating-point algorithms into fixed-point DSP processors under accuracy constraint has been proposed and a tool has been developed in the case of DSP. The results have been presented in [26].

Our aim is to extend this methodology for hardware implementations and more particularly for FPGA architectures. This style of architecture allows more flexibility with regards to word-length optimization since the architecture has to be synthesized. This work is a part of the OSGAR RNTL project whose aim is to develop high-level tools for designing reconfigurable architectures. A methodology which allows to minimize the architecture area under a computation accuracy constraint has been proposed. To obtain an optimized specification, the conversion process is coupled with the architecture synthesis process. The tool for the fixed-point conversion is under development and will be coupled with our high-level synthesis tool BSS.

### *6.2.5. Fixed-point accuracy evaluation for non-linear systems*

**Participants:** Daniel Menard, Romuald Rocher, Pascal Scalart, Olivier Sentieys.

An important part of the floating-point to fixed-point process is the fixed-point specification accuracy evaluation. The goal is to extend our previous works to obtain an analytical accuracy evaluation method for all kind of systems. More particularly, the adaptive systems are under consideration. The results for non-linear and non-recursive systems have been published in [25].

A general model has been developed for adaptive filter based on the gradient algorithm. The expression of the output quantization noise power has been proposed for the different variants of the LMS algorithm [28] (classical LMS, NLMS, Leaky LMS) and the APA algorithm. The APA algorithm was introduced in 1984 but no fixed-point study has ever been published. This algorithm converges faster than the variants of the LMS algorithm and this convergence time is independent of the input signal statistical parameters.

Our work is focused on the study of the output quantization noise power for non-linear recursive systems. Two models have been proposed. The first model which do not take into account the correlation between the signal allows to obtain a simple analytical model. The second model which is more complex and based on the recurrence unrolling leads to more accurate results. Our models are valid for the different quantization laws (truncation and rounding). The model quality has been evaluated by comparing our estimation with the results obtained by simulations.

### *6.2.6. ARMOR architecture description language*

**Participants:** François Charot, Ludovic L'Hours.

Our research aims at developing methods to model programmable processors through their instruction sets and tools to derive software development environments from these processor models. A processor description in ARMOR is a grammar whose each derivation is a possible behavior of the instruction set. ARMOR thus describes the behavior of the instruction set, including its semantics, temporal information, the use of the resources, as well as the possibilities of parallelism at the instruction level. Extensions added to the language allow the control of the processor to be expressed [19]. Future works concern the generation of SystemC simulation models of processors from ARMOR models.

### 6.2.7. System modelling for dynamically reconfigurable architectures

**Participants:** Imène Benkermi, Didier Demigny, Daniel Chillet, Sébastien Pillement, Olivier Sentieys.

SoC platforms including dynamically reconfigurable units aim at supporting complex multimedia applications using a real-time operating system. They consist in different execution modules, i.e. general-purpose processor(s) and specialized/reconfigurable accelerators including the DART dynamically reconfigurable architecture. They heterogeneity led to a specification by means of the three following levels of description: software, middleware and hardware. Each level corresponds to a task configuration on the platform. Hence, the operating system has to ensure specific services imposed by the reconfigurable aspect; namely, ensuring task communication and migration between the three levels of description.

The software model describes the different tasks of the application supported by the architecture platform. A UML-based modelization has been used. In addition to the task characteristics, real-time constraints and links between tasks, this modelization permits to specify the different forms a task can have depending on the target it will eventually execute on. This work has been done through a collaboration with the ETIS (Cergy-Pontoise) and LESTER (Lorient) laboratories.

We are working on an on-line scheduler able to distribute the task set on the different computing units, while meeting their real-time constraints and taking into account their heterogeneity; i.e. one task may have different execution times depending on the unit it will execute on. Simulations of multimedia application on platform prototype based on these specification models are to be conducted.

## 6.3. Study of applications

**Keywords:** *WCDMA, biomedical, cryptographic applications, image indexing, mobile telecommunication, speech processing.*

Applications stemming from third-generation radio-communication systems are good candidates for the study of hardware systems mixing programmable parts executing software code and specialized modules dedicated to the acceleration of time consuming parts of applications.

Data filtering, speech processing are also under consideration.

### 6.3.1. 3G mobile application prototyping

**Participants:** François Charot, Michel Guitton, Daniel Ménard, Madeleine Nyamsi, Patrice Quinton, Taofik Saïdi, Pascal Scalart, Olivier Sentieys, Charles Wagner.

WCDMA is typically considered as one of the most critical application of next-generation telecommunication systems. The main idea of WCDMA (Wideband Code Division Multiple Access) is to share the communication support between several users by scrambling user symbol with a pseudo-noise code. This access technique adapts the signals to the communication support by spreading its spectrum.

A WCDMA communication chain (transmitter and receiver) was specified using Matlab. This chain constitutes the reference version for the application implementation. A WCDMA receiver demonstrator has been developed. The different digital parts of the baseband receiver have been implemented in the Altera development board based on the Stratix FPGA from Altera. This receiver includes the FIR receiving filter, the searcher, the synchronization, the canal estimation and the symbol decoding. The input signal is generated by the Rhode & Schwartz AMIQ generator. This development allows to analyze the architecture area for different fixed-point specifications.

Irisa has acquired[13] a prototyping platform[14] that allows applications described using Simulink to be executed on a special-purpose board including a DSP processor and a FPGA chip (SignalMaster platform from Lyrtech. We have implemented a simplified WCDMA emitter-receiver on this platform, and we have studied the performance of the various blocks of this application on this platform, including a filter that was generated using MMAlpha. This research [20] is a preliminary step in the study of fast estimation techniques for the design of SoC.

[13] Thanks to a Bonus-Qualité-Recherche grant of the University of Rennes 1.

[14] http://www.lyrtech.com/DSP-development/dsp_fpga/signalmaster.php

### *6.3.2. Next generation MIMO mobile communication systems*

**Participants:** Taofik Saïdi, Pascal Scalart, Olivier Sentieys.

Multimedia services, which are expected to dominate wireless communications in near future, demand enhanced data throughput for both uplink and downlink directions. Multiple-Input Multiple-Output (MIMO) techniques hold the potential of dramatically increasing the data rates and spectral efficiency of wireless communications systems. They provide solution to two fundamental problems in wireless communications, the limited spectrum resource and the hostile transmission medium of fading channel. MIMO is still in a starting phase in different standardization bodies for radio communications and is well suited for 4G standards.

This project is a joint research program between the *Laboratoire de Radiocommunication et de Traitement du Signal* (LRTS) at Laval University (Canada) and R2D2. It concerns the efficient implementation of novel MIMO algorithms adapted to the W-CDMA context, and is firstly focused on a $2 \times 2$ MIMO W-CDMA link [17].

The two antennas transmit independent bitstreams, each one being spread by a different channelization code. The use of orthogonal codes permits to identify the source (transmit antenna) of the different received signals. At the receiver, the UMTS standard matched filter is applied. The filtered signal is applied to a searcher block which performs the finger (path) search in the wideband impulse response. It transmits the position of each finger to the RAKE blocks developed in our previous works. A RAKE block performs channel estimation, despreading and compensation effects. The outputs of the RAKE blocks are sent to a MIMO decoder which performs self-interference cancellation.

The entire reference model has been developed in Matlab and some blocks have been implemented in the FPGA. A Simulink Model is being developed to target a Lyrtech SignalMaster Platform (DSP/FPGA board) and a C model for high-level synthesis. Implementation results in a Xilinx Virtex-2000E FPGA show that the matched filter (64 taps) requires 3% of the LUTs (look-up tables) while one complete finger requires 7%.

### *6.3.3. RDISK: Reconfigurable DISK*

**Participants:** Steven Derrien, Ludovic L'Hours.

The Reconfigurable DISK, is a joint project between the Symbiose and R2D2 teams, that has been funded by the French Research ministry during the last years.

Its goal is to develop a specialized architecture following the *smart disk* concept. The idea is to attach reconfigurable computation capabilities near the disk for providing on-the-fly data filtering to speed-up large database scanning. The target application field is genomic data extraction, and a 48 disk prototype is currently in use.

The team R2D2 is involved in the design, implementation and validation of the RDISK Programmable System-on-Chip, which is based upon a Xilinx FPGA. The goal was to provide a small foot-print (in terms of resource usage) SoC. Among other tasks, this project included the design of a SoC bus arbiter, of a high-performance SDRAM controller and of an ATA/IDE hard drive controller. A significant amount of work has also been done on the design of a light-weight operating system layer, whose purpose is to handle the RDISK dynamic reconfiguration capability and to provide simple communication primitives between the host and the boards. All these contributions have been successfully tested on the system, and now serve as a framework for all other RDISK project participants.

### *6.3.4. Noise Reduction in Speech Processing*

**Participant:** Pascal Scalart.

In this study, we focus on the problem of single microphone speech enhancement in noisy environments. Common short-time noise reduction techniques proposed in the art are expressed as a spectral gain depending on the a priori SNR. In the well-known decision directed approach, the a priori SNR depends on the speech spectrum estimation in the previous frame. As a consequence, the gain function matches the previous frame rather than the current one which degrades the noise reduction performance. To counteract this problem, we proposed a new system called Two-Step Noise Reduction (TSNR) technique [27] which solves this problem

while maintaining the benefits of the decision-directed approach. The a priori SNR estimated in the first step provides interesting properties but suffers from a delay of one frame which is removed by the second step of the TSNR algorithm. So, this technique has the ability to immediately track the non-stationarity of the speech signal without introducing musical noise effects. In addition, in automatic speech recognition application, the TSNR algorithm exhibits a significant reduction of substitution and insertion errors leading to a substantial relative recognition performance improvement. The ETSI STQ Aurora working group has selected this advanced feature extraction algorithm for distributed speech recognition for mobile and Internet based applications.

# 7. Contracts and Grants with Industry

## 7.1. IST Ozone (2002-2004)

**Participants:** François Charot, Madeleine Nyamsi, Patrice Quinton, Charles Wagner.

The IST Ozone project (*New Technologies and services for emerging nomadic societies*) began in November 2001. It gathers the following partners: Philips Electronics (Netherlands), Imec (Belgium), Epictoid (Netherlands), Eindhoven University of Technology (Netherlands), INRIA, Thomson Multimedia (France).

The Ozone project aims at investigating, defining, implementing and integrating a generic platform for ambient intelligence applications. This project aims at making more convivial the interactions of the user with the equipments and the applications to allow new services of better quality. One of the research orientations relates to hardware architectures on which can be implemented the ambient intelligence.

The object of the work undertaken by the team relates to the definition and the design of a methodology aiming at implementing a complex SoC architecture combining processors and dedicated hardware accelerators on a FPGA based architecture. For parts of the application requiring high-performance, highly parallel designs exploiting the regularity of computation are mandatory. The MMAlpha system focuses on exploiting this regularity, it allows parallel and regular architectures to be derived for the most compute-intensive parts of programs that is to say loops. The rest of the algorithm is executed in software on processor cores (which may be very specialized processors in the case of ASIP) designed with Calife, an experimental platform for retargetable code generation designed to satisfy the constraints of architecture exploration and the concurrent design of the processor and its compiler.

## 7.2. Architectures based on multiple-valued logic for telecommunication applications (2001-2004)

**Participants:** Daniel Chillet, Hélène Dubois, Ekué Kinvi-Boh, Sébastien Pillement, Olivier Sentieys.

Until the development of the SUS-LOC technology by E.D. Olson, the MVL techniques were not realizable in practice and remained only theoretical. This technology makes it possible to fulfill any MVL function with a complexity equivalent to CMOS technology in the binary case and uses standard circuits foundries. The international patent protecting it was classified like one of the most innovative of these last years by the US Patent Office.

An active research collaboration was established with EDO LLC, the american company founded by D. Olson, for the study and the development of new systems using the MVL, in particular in the field of DSP for telecommunications.

## 7.3. OSGAR (2003-2005)

**Participants:** Daniel Chillet, Nicolas Hervé, Daniel Menard, Sébastien Pillement, Olivier Sentieys.

OSGAR is a RNTL project, gathering the following partners: CEA-list, TNI-Valiosys, the university of Western Brittany, and R2D2.

This project aims at studying and developing tools for high-level synthesis able, starting from C code, semi-formal specifications or object code, to carry out an automatic migration towards one or more reconfigurable circuits. The object of the work undertaken by the team relates to the following points.

- the adaptation of the tools of the circuit design BSS software platform to reconfigurable architectures, in order to take into account in an automatic way the data coding and the size of the operators. To ensure this point, we need to define more precisely an exchange format between the different tools provided by the partners of this project. An XML application has been defined and new interfaces have been added to each tool. This point has been demonstrated during the RNTL days in October (4-5 October in Rennes).
- the modeling of reconfigurable architecture from the point of view of the developed software tools. The objective is to integrate in the models the power consumption aspects. The goal is to be able to provide estimates of power dissipated during prototyping.
- the validation by the implementation of two applications (image processing, WCDMA) on the various architectures considered in the project.

# 8. Other Grants and Activities

## 8.1. National initiatives

The team R2D2 participates to the activities of two multi-laboratory team of RTP (Pluridisciplinary Thematic Network) SoC of the CNRS): Pomard and SocLib. R2D2 members take part to the specific action *Low Power Design* (AS106).

The team R2D2 participates to the activities of:

- GdR-PRC ISIS (*Information Signal ImageS*), working group GT7 *Algorithms Architectures Adequation*.
- GdR-PRC ARP (*Architectures Réseaux et Parallélisme*), working group *Specialized architectures*.

### *8.1.1. ReMiX: Reconfigurable Memory for Indexing Huge Amount of Data*

**Participants:** Gilles Georges, Steven Derrien, François Charot.

Indexing is a well-known technique that accelerates searches within large volumes of data such as the ones needed by applications related to genomics, to content-based image or text retrieval.

The ReMiX project proposes the design of a dedicated and very large index memory (several hundred of Giga-bytes, distributed among a cluster of nodes), big enough to entirely store huge indexes and avoid the use of any disk.

In addition, the index memory uses reconfigurable hardware resources to tailor – at the hardware level – the memory management to best support the specific properties of the indexing schemes. It also offers the opportunity to implement algorithms having potential parallelism.

An hardware platform based on Flash memory technology is being developed by the R2D2 team. The platform consists of several computing nodes connected through a high performance network interface. Each node is based on a Xilinx FPGA processing element coupled to 64 Gbyte of Flash memory. This approach allows to combine the benefits of hard-drive storage (non-volatility, density), with those of memory (bandwidth, access time) to efficiently support large indexed databases.

This three-year project (October 2003 - September 2006), coordinated by the Symbiose project, is funded by the French ministry (ACI Data Mass program). The team R2D2 is strongly involved in the design of the hardware platform.

## 8.2. International bilateral relations

### *8.2.1. Europe*

R2D2 cooperates with the University of Leiden in the Netherlands (Ed Deprettere) on parallel architecture synthesis.

R2D2 cooperates with UCL at Louvain-La-Neuve on the topic of ternary technology integrated circuits. A prototype circuit is under development with the SOI technology of the micro-electronics laboratory (DICE of UCL).

R2D2 cooperates with Lund University (Sweden) on Constraints Programming approach applied to the reconfigurable systems synthesis flow.

R2D2 cooperates with the university of Girona in Spain (Computer Vision and Robotic Group of the Institute for Informatics and Applications) on parallel architectures for vision algorithms applied to underwater robot.

### *8.2.2. Africa*

R2D2 cooperates with ENIT in Tunis on the topic of mobile telecommunication architectures.

R2D2 cooperates with the university of Antanarivo and the Polytechnic Superior School of Antananarivo in Madagascar, for the training of faculty member.

### *8.2.3. North America*

R2D2 maintains relations with the computer science department of the University of Colorado State in Fort-Collins on the development of MMAlpha.

R2D2 cooperates with the LSSI laboratory of Trois-Rivières university in Québec, on the design of architectures for filters.

R2D2 cooperates with Los Alamos National Laboratory on optimized reconfigurable architectures synthesis.

R2D2 cooperates with the LRTS laboratory of Laval university in Québec on the topic of architectures for MIMO systems.

## 8.3. Visiting scientists

- Ramamonjy Andrianivosoa (Polytechnic Superior School of Antananarivo, Madagascar) from 05/02/2004 for 1 month.
- Viorela Ila (University of Girona, Spain) from 09/06/04 for 2 months.
- S. Mathieu and S. Roy (University of Laval, Québec) from 10/22/2004 for 2 weeks, I. Laroche and J. Veilleux (University of Laval, Québec) from 10/01/2004 for 4 weeks.

# 9. Dissemination

## 9.1. Activities in the scientific community

F Charot is steering committee member of the SoC Pluridisciplinary Thematic Network (RTP SoC), set up at the department STIC of the CNRS.

S. Pillement served as technical program committee member for *14th International Conference on Field Programmable Logic and Application FPL*, 2004.

P. Quinton is member of the steering committee of the System Architecture MOdelling and Simulation (SAMOS) workshop.

C. Wolinski was General chair of the 30$^{th}$ Euromicro conference and Digital System Design conference (DSD'04). He gave a tutorial on *Reconfigurable Computing* at DSD'04. He was a member of technical committee of DSD'04.

## 9.2. Teaching and responsabilities

D. Chillet teaches a course on *advanced processors architectures* in Master STIR.

H. Dubois is the associate academic director at Enssat.

M. Guitton is in charge of the communication at Enssat.

L. Perraudeau was the associate director of Ifsic, until 05/15/04 (responsible for the budget and the equipment). He is responsible for a course on the object languages in the DESS Isa (Computer science and its applications) of the university of Rennes 1, teaches the design of integrated circuits in DIIC second year), and teaches in Licence d'informatique, in Deug Sciences, mention SM and STPI.

P. Quinton is responsible for the parallel algorithmic course (Alpa module) in the Master in computer science of the university of Rennes 1, teaches in Deug Sciences, mention SM and STPI, and in DIIC (second and third year). Since september 2004, P. Quinton is deputy-director of Ecole Normale Supérieure de Cachan, responsible of the Brittany branch of this school.

O. Sentieys is responsible for a signal and architecture module of the Master STI of the University of Rennes 1 and the DRT in electronic of Enssat. He teaches at Enssat and gives courses on *Methodologies for integrated system design* in Master STI and on *Low-power digital CMOS circuits* at Enst de Bretagne.

C. Wolinski is responsible for Computer Organization and Architecture branch in DIIC. He is responsible for the following courses: CSE *Design of Embedded Systems* (DIIC), SIA *Signal, Image, Architectures* (DIIC), XAA *Advanced Architectures* (Magister).

Graduate student intern: Seila Nuon, Benoît Houyère (Ifsic, France).

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