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INSTITUT NATIONAL DE RECHERCHE EN INFORMATIQUE ET EN AUTOMATIQUE

Team R2D2

Reconfigurable and Retargetable Digital Devices

Rennes

THEME COM

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2. Overall Objectives

2.1. Introduction

The problems tackled by the team R2D2 relate to the design of specialized systems on reconfigurable platforms. A hardware platform is a structure of Integrated Circuits (IC) containing a set of programmable components –general purpose or specific processor cores–, memories and generally specialized components. Such a platform can be seen as an integrated architecture scheme, common to numerous algorithms belonging to a given application domain. This notion is the answer given by the designers of embedded systems to the increasing difficulty they have to implement their applications [50]. One can consequently imagine that in the future, most of the ICs necessary to the design of a complex system will be derived from a given existing platform. This design approach is an alternative to the IP-based (*Intellectual Property*) design approach, in which the system is built by assembling separately designed components. A reconfigurable platform includes a set of reconfigurable components (blocks of reconfigurable logic, reconfigurable data-path, flexible communication networks). In terms of area and power consumption, the reconfigurable resources enable a far more efficient use of the silicon than in programmable processors or in specialized components.

Future platforms will be highly parallel, heterogeneous, programmable and reconfigurable. Parallelism is the only way of reaching the performance level required by future applications. Heterogeneity results from the report that an efficient design is often composed of several subsystems, characterized by well-differentiated computation requirements. Programmability avoids freezing the functionalities. Finally, reconfigurability combines the speed of specialized solutions and the flexibility of traditional programmable components.

Our scientific objectives seek to profit from various methods (very high-level synthesis, behavioral synthesis, flexible compilation, floating-point to fixed-point conversion, etc.), contributing each one with its specificities, to the design of a part of a specialized system. The models and the underlying techniques allow the use of estimators, thus contributing to the choices of implementation, with a precise knowledge of the performance of the system, of its complexity and its power consumption.

2.2. Directions

Research undertaken within the team R2D2 aims at facilitating the design of reconfigurable hardware systems, by proposing models of architectures and associated design methodologies which favor the adequacy between the algorithms of the applications and the architectures supporting the implementation. The team links together three main directions.

2.2.1. New architectures and technologies

Our studies, motivated by the constraints of high-performance, flexibility, and low-power consumption, focus on the following topics:

- new organizations of reconfigurable structures offering the speed of specialized solutions and the flexibility of traditional programmable components with regards to application areas like mobile telecommunications ;
- the application of advanced mobile telecommunication techniques to the design of Network-on-Chip (NoC) ;
- architectures for low-power sensor networks ;
- Multiple-Valued Logic (MVL) circuits and architectures.

2.2.2. Modeling, synthesis and compilation targeting reconfigurable platforms

The implementation of an application on a reconfigurable platform requires a large set of techniques. Successive refinements lead to the implementation choices of the various parts of the application on the components of the platform. Our studies focus on the following aspects: SoC modeling, synthesis of dedicated hardware accelerators, processor modeling and flexible compilation, floating-point to fixed-point conversion.

2.2.3. Study of applications

Third and fourth-generation mobile telecommunications are our privileged field of applications. Moreover other application domains are considered: cryptography and traffic filtering in high-speed networks, image indexing, speech processing. Our research include the prototyping of applications on reconfigurable and programmable platforms.

3. Scientific Foundations

3.1. Panorama

R2D2 research activities inherit from two scientific communities working on connex areas in the design of hardware systems: the first relates to methods and tools for specialized architecture design and the second concerns signal processing and dedicated circuit architectures. We first outline the evolution of specialized architectures. Then we give some bases of our research.

3.2. New architectures and technologies

Keywords: *Network-on-chip*, *SoC*, *computation grain*, *low-power consumption*, *multiple-valued logic*, *reconfigurable architecture*, *sensor network*.

By the end of the decade, IC technology should allow to fabricate billion transistors chips, instead of few tens of millions today as illustrated by the document published by the SIA[1] (*Semiconductors Industry Association*). The hardware systems of the future equipments will be miniaturized – one now usually speaks about System-on-Chip (SoC) – while mixing architectures which will be highly heterogeneous and will include dedicated hardware accelerators.

Even if electronic CAD tools and associated design methodologies progressed much during last years, the design of new ICs has not become easier. On the contrary, the gap between the capacities offered by the IC technology and the potential of the current design tools – the famous *technology gap*, – has never been as large. A rather fundamental change in the way of designing circuits is needed.

This evolution of the technology has an impact on the architectures of manufactured ICs. With the years, a migration is noted: from ASIC towards SoC, and in an immediate future towards reconfigurable programmable platforms.

- ASIC were prevalent between 1980 and 1995, and from now on are only used as particular blocks in more complex heterogeneous systems.
- The first SoCs were designed around 1995. Thanks to the increasing density of chips, a complex SoC usually integrates one or more processor cores (general purpose processor or digital signal processor), memory blocks (RAM, ROM, flash memory, EPROM, etc.), as well as many different interfaces useful for the correct working of the system. They combine hardware and software components. Their design relies on the use of synthesis, place and route tools, and libraries of reusable components.
- In the near future, SoC will evolve to platforms, which are structures of integrated architectures, common to a set of algorithms or applications belonging to the same field of applications. The design tools and methodologies must thus make it possible to design a specialized architectures starting from this basic architecture [58]. The platforms will allow the needs for a broader spectrum of applications to be satisfied, at the price of a reduction of the variety of designed circuits.

Associating flexibility with high-performance and energy efficiency, is a critical issue for embedded applications. This is particularly true for mobile applications. These three constraints are taken into consideration in our architecture studies.

[1] http://www.itrs.net/Links/2005ITRS/Home2005.htm

3.2.1. New reconfigurable architectures

These last years saw the emergence of new reconfigurable architectures [46], which are an alternative to the traditional performance/flexibility compromise, conditioning the choice between purely hardware (ASIC) or purely software (programmable processor) solutions. For an application domain like mobile telecommunications, three main constraints have to be combined: high-performance, low-power consumption and flexibility. Computation grain, reconfiguration schemes, are open research topics.

As an example, the Pleiades [56] project is an architectural platform supporting several computation grains – logic operations are treated as effectively as the arithmetic operations, – designed in order to consume a minimum of energy whatever the level of required performance. However, this platform does not make it possible to support the set of constraints previously discussed because of the static feature of its reconfiguration which limits it to certain field of applications, the coding of words having been the support of the study.

In addition to these two examples, many reconfigurable architectures are based on FPGA-type circuits and the majority of them, such as GARP [48], NAPA [57], Chimaera [47], integrate a traditional programmable processor in charge of the sequencing of the treatments on the reconfigurable block. Other architectures such as Piperench [43] or RaPiD [35] can be reconfigured at a higher level, respectively at the operator and functional level. The concept of computation grain indeed constitutes an interesting and significant research subject. The majority of the FPGA circuits are *fine grain* since they can be reconfigured at the bit level, which contrasts with programmable processors that manipulate words (32-bit words for a number of them). When bit-level reconfiguration is not required by the application, coarse-grained structures must be built starting from the elementary blocks of the reconfigurable structure, which results in a over-cost of the circuit. To limit this over-cost, new coarse-grained reconfigurable architectures are proposed. This results in structures in which the elementary blocks correspond to arithmetic logic units, multipliers, memories, etc. In addition to Piperench and RaPiD already mentioned, the architectures Matrix [39] at MIT, MorphoSys [54] at the University of California at Irvine, can be quoted. And among the commercial realizations: the array of reconfigurable arithmetic logic units of Elixent, and the XPP processors of PACT[2].

3.2.2. Network on Chip design

The rapid growth of device densities on silicon has made it possible to deploy complete systems (SoC) using validated IP blocks. Traditional common interconnection resource is a shared bus. Increasing the number of blocks connected on this bus emphasizes the limitation of this solution. Among those limitations stand the increasing noise sensibility and the scalability of the interconnection scheme. In order to precisely control the electrical and scalability parameters [36] of the interconnect, in-chip communications have to be organized. A new paradigm is rising to face the interconnect issue [34]. The Network on Chip (NoC) concept proposes to use well-defined network layers to build the interconnection scheme. It separates the communication process into three different layers which provide the other layers with services (error detection or correction, routing or packetizing for example). A NoC is dedicated to the reliable and efficient routing of information grouped in packets (with redundancy information, routing information, etc.).

Assuming that the voltage swing on wires will decrease in the next few years, the reliability of the physical layer will decrease. The challenge is to provide a reliable, efficient and low-power link to meet the requirements of future SoCs.

3.2.3. Wireless sensor networks

Wireless sensor networks are groups of sensors interconnected with each other through wireless links. The aim of these sensor networks is to collect information from the area and to relay it through the network. Sensor networks have raise neww challenges in wireless communications [62]. First, the autonomy or the lifetime of a sensor network must be very high, since the sensors can be integrated in concrete, in the soil or even in the body of living beings where the replacement of the batteries is impossible or difficult. Energy-scavenging techniques can be used for that purpose. Then, these networks have to be self-organize since they have to cope with local sensor breakdowns, for example when some sensors run out of power. Another important

[2] http://www.pactcorp.com/

singularity is the fact that the data rate needed by the applications should be quite low, since the data does not have to be sent continuously, but only when changes occur. Many applications have been proposed, in miscellaneous domains of activities, e.g. in agriculture, building, bridges, transport, military applications, enemy monitoring, chemical and bacteriological monitoring, emergency after earthquakes. Many wireless systems already exist and are commercially successful. Their specifications have generally been developed in order to maximize the spectral efficiency. In sensor networks, the energy is more critical than the available spectrum. For these kind of applications we should rather maximize the power efficiency than the spectral efficiency. A communication system can be described functionally by dividing the processing in layers. The OSI (Open Systems Interconnection) model describes seven layers for the processing. The problem is that the design of a communication system cannot efficiently be done for each layer separately because layers are coupled to each other. Separate optimizations for each layer is not sufficient. That is why designing a power-efficient system must take into account this coupling, by making cross-layer optimizations [42]. For that reason, it is better to consider few layers.

We worked with a fragmentation of the protocol stack in only two layers. The higher-level part includes the aims of OSI application, presentation, session, transport, and network levels. The lower-level part includes the aims of OSI data-link and physical levels. The lower-level part considers a transmission between two neighbor nodes and has to optimize the communication from this point of view. The higher-level part considers a transmission between generally distant applications, assuming that the lower-level communication used are energy-efficient.

This fragmentation has already been used in [60], and can be justified by saying that networking issues are coupled together only in the higher-layer part, while the channel management issues are coupled only in the lower-layer part.

3.2.4. Multiple-Valued Logic (MVL) architectures and circuits

Nowadays, numerical systems are exclusively based on a binary representation of numbers and computations. It was shown that the use of a higher number of logical states can reduce the number of interconnection wires and the memory area [40]. It also optimizes the arithmetic processing.

ICs performances are limited by complex wiring –a great amount of the chip performance is devoted to interconnection–, large propagation delay and high-power consumption. Using Multiple-Valued Logic (MVL) techniques, the amount of interconnections and the power consumption caused by important switching activity on each node of a circuit can be reduced. The SUpplementary Symmetrical LOgic Circuit structure (SUSLOC) is a new promising approach for the implementation of MVL functions in voltage-mode. It combines low-energy consumption and a speed equivalent to binary CMOS structures.

3.3. Modeling, synthesis and compilation for reconfigurable platforms

Keywords: *ASIP*, *IC*, *architecture description language*, *data coding*, *design methodology*, *fixed-point arithmetic*, *flexible compilation*, *high-level synthesis*, *parallel architecture*, *precision*, *retargetable compilation*, *specialized processor*.

3.3.1. Dedicated hardware accelerator synthesis

Although the architecture of ICs evolves to increasingly programmable and reconfigurable solutions, future silicon systems will continue to integrate specialized hardware components. The design of such components rests on the use of synthesis techniques.

Today circuits synthesis starts from high-level specifications. The specification of programs carrying out regular computations in the form of recurrence equations allows powerful static analyses and transformations of programs for the derivation of regular architectures [4].

The base of our research is the polyhedral model, which is well-suited to the expression of the calculation parts applications and which allows the expression and the handling of systems of recurrence equations.

There exist many academic environments prototypes for the automatic synthesis of specialized architectures starting from high-level specification: for example, Diastol, Presage, Hifi, Cathedral, Sade, PEI and MMAlpha. Tools performing a high-level synthesis from the C language now exist on the market: tools based on SystemC[3] like *CoCentric SystemC Compiler*[4] of Synopsys, *A|RT Builder* of Adelante Technologies/Frontier Design, tools based on C and its extensions as *Celoxica DK1 Design Suite* [5] of Celoxica.

Few tools rest on a true parallelization but many research projects explore this approach: Flex[6] and Raw[7] at MIT, Piperench[8] at Carnegie-Mellon, Garp[9] at Berkeley, Pico [59] at HPLabs Palo Alto, Compaan[10] in Leiden.

Among these tools let us cite Alpha [6] and MMAlpha, initially developed in the project-team Cosi, evolved from Diastol and constitute today a practical environment for the handling of recurrence equations and the high-level synthesis of dedicated hardware accelerators. We are continuing to make evolve MMAlpha. The work is done in close cooperation with the CompSys team (LIP, ENS Lyon).

3.3.2. Processor modeling and flexible compilation

Hardware description languages like VHDL or Verilog are largely used to model and simulate processors, but mainly with the aim to design hardware. The design of SoC requires methodologies and tools for the exploration of the architecture design space. This exploration requires the use of architecture description languages (ADL), adapted to the specification of the SoC architecture models. Very early in the design process, ADL play a role for the validation of SoC architectures, and also for the automatic generation of the software development tools necessary to the software and hardware design of the architecture.

Most of the existing architecture description languages aimed at the specification of processor architecture, privileging either the synthesis, or the generation of compilers, or the generation of simulators. None of the existing languages is really directed towards architectural exploration.

In the category of architecture description languages mainly directed towards processor hardware synthesis, one can quote Mimola, developed at the university of Dortmund, and used to describe target machines in the MSSQ and Record [53] compilers. Mimola is very close to hardware description languages like VHDL or Verilog. A Mimola description can be employed for the synthesis, simulation, and code generation, after extraction of the instruction set.

With regard to the architecture description languages mainly directed towards compilation, one can quote nML, designed at the university of Berlin, ISDL proposed by the MIT, MDES developed at the university of Illinois, Expression developed at the University of California at Irvine.

With regard to the architecture description languages mainly directed towards simulation, one can quote LISA [55], developed at the university of Aachen. LISA allows the generation of cycle-accurate simulators for DSP processors. Both the structure and the behavior can be modeled.

The existing architecture description languages can also be classified according to the modeling level: behavioral or structural. A language like Mimola is of structural level, languages like nML and ISDL are of behavioral level. LISA, Expression and MDES mixes the two levels of modeling.

There is no standard as regards architecture description languages. The ARMOR language developed in the project-team Cosi, constitutes a practical approach for the modeling of complex architectures. It is suited to architectural exploration and automatic generation of software development tools (compiler, simulator, processor design tools, etc.). .

[3] http://www.systemc.org
[4] http://www.synopsys.com/products/cocentric_studio/
[5] http://www.celoxica.com/products/tools/dk.asp
[6] http://flex-compiler.lcs.mit.edu
[7] http://cag.lcs.mit.edu/raw
[8] http://www.ece.cmu.edu/research/piperench/
[9] http://brass.cs.berkeley.edu/garp.html
[10] http://www.liacs.nl/~cserc/compaan/index.html

3.3.3. Floating-point to fixed-point conversion

The efficient implementation of an algorithm on a specialized processor, such as for example a DSP (Digital Signal Processor) or an ASIP (Application Specific Instruction-set Processor), or on a hardware structure, such as an ASIC or a FPGA (Field Programmable Gate Array), requires for reasons related to cost, consumption or silicon area constraints, the use of fixed-point arithmetic, whereas the algorithms are usually specified in floating-point arithmetic. This conversion is a tiresome task and error-prone if it is carried out manually. Indeed, some experiments [44] showed that the time devoted to this conversion step is relatively significant, manual conversion being able to represent up to 30% of the total time necessary to the implementation of the algorithm. Let us note in addition that the time-to-market constraint requires the use of high-level development tools, allowing to automate certain tasks.

The existing methodologies for fixed-point data automatic coding [51], [61] carry out a transformation from floating-point data representation into a fixed-point representation, without taking into account the architecture of the target processor. However the analysis of the influence of the architecture on the precision of computation and the various phases of the code generation shows the need for taking the architecture features into account and for coupling the coding and code generation processes to obtain an implementation of quality in terms of precision of calculations and execution time.

Data coding optimization must be carried out under precision constraint, and it is thus necessary to determine the signal-to-quantization noise ratio (SQNR) of the application. The SQNR determination methods [49] are generally based on simulation. But within the framework of the data coding optimization these methods use an iterative process leading to high times of optimization. The study of analytical techniques offers new perspectives for the accuracy evaluation.

4. Application Domains

4.1. Panorama

Third- and fourth-generation mobile telecommunications is our privileged field of applications. In the framework of research and/or contractual cooperations, other application domains are therefore considered: image indexing, traffic filtering in high-speed networks, and speech processing.

4.2. Mobile telecommunications

The future generations of telecommunications constitute a privileged field of applications for IC designers because of the diversity of the constraints to be satisfied. Very high-level of performance – superior to 12 billion operations per second – is required as the result from the association of multimedia capacities and access techniques such as the WCDMA (known as 3G). Flexibiliy and programmability is needed in order to support the whole of the algorithms integrated into the standards of present generations (GSM, DEC, IS-95) and their evolutions.

From the point of view of hardware architectures, the next generation systems will have to deal successively with very different applications. Indeed, the common tasks in a third-generation communication chain manipulate variable data sizes according to *distance* separating the task from the transmitter or the receiver, – the application tasks handle data of high-granularity such as images whereas the tasks giving access to the transmission operate on bit-level data. Because of the importance of the application spectrum integrated into the future telecommunication standards, the computation treatments to be applied to these data will also be very diversified, which will result in very different calculation patterns. Even if each one of these constraints can be supported, combining them is challenging. Moreover the time-to-market constraints impose the definition of development tools as portable as effective. Current architectural solutions does not offer practical solutions for energy aware products (lower than 500mW in peak).

5. Software

5.1. Panorama

Keywords: *library*, *polyhedral computation*.

Research undertaken by R2D2 is in the context of software and hardware tools for the design of hardware systems. In order to promote the studied techniques, several software prototypes are developed (Polylib, MMAlpha, BSS, ARMOR/CALIFE). Among those, four distributed software are presented: Polylib an *open source* library of calculation on polyhedron, MMAlpha for the high-level synthesis, BSS a platform for the design of circuits and Gecos a flexible compilation platform.

5.2. PolyLib

Keywords: *ASIC*, *CAD*, *architecture synthesis*, *data parallelism*, *functional programming*, *polyhedral computation*.

Participants: Patrice Quinton [contact], Tanguy Risset [CompSys, INRIA Rhône-Alpes].

The polyhedral Polylib library, developed in C, is an *open source* library of calculation on convex polyhedron. It was initially developed by Hervé Le Verge and Doran Wilde at INRIA Rennes. It is today maintained and developed with the LIP (ENS Lyon) and the ICPS (university of Strasbourg). The handling of the domains used in the recurrence equations or spaces of indices described by nested loops justifies the use of such a library. This library is currently used (independently of MMAlpha) by several research organizations (in England, the United States, the Netherlands, and in France).

To know some more, refer to http://www.irisa.fr/cosi/polylib/user/ or contact Patrice Quinton.

5.3. MMAlpha

Keywords: *ASIC*, *CAD*, *architecture synthesis*, *data parallelism*, *functional programming*.

Participants: Patrice Quinton [contact], Tanguy Risset [CompSys, INRIA Rhône-Alpes].

MMAlpha implements transformations on the Alpha language. The Alpha language was proposed by Christophe Mauras [6]. The implementation is carried out in the Mathematica language (from where the name MMAlpha) and is built on the Polylib library.

Alpha program transformations are implemented by combining the Mathematica language and the Polylib library. The principle is to derive either an architecture, a sequential or a parallel code starting from an algorithmic specification of a problem. These transformations are semi-automatic, i.e. the actions to be performed are indicated by the user but the transformation itself is carried out by MMAlpha. Automatic transformations are also available, and provide in some cases satisfactory results.

The design methodology is inherited from the method of systolic array synthesis. This field is studied from the theoretical point of view, and results of these research are implemented and experimented in the MMAlpha software. This software makes it possible to test various existing synthesis strategies, to study various possibilities of parallelization and to generate an architectural description of a circuit thanks to the AlpHard format (subset of the Alpha language). The interface between MMAlpha and logic synthesis tools is done thanks to a translation towards VHDL.

The software was the implementation support of many theses carried out at Irisa. It is used by several research teams within the framework of collaborations with R2D2. It is one of the only tools making it possible to describe an algorithm and its hardware implementation in the same language and to deduce this implementation with proven transformations.

To know some more, contact Patrice Quinton.

5.4. BSS, BOOST

Keywords: *architecture synthesis*, *circuit design*, *low-power consumption*, *placement*.

Participants: Daniel Chillet [contact], Sébastien Pillement, Olivier Sentieys.

The BSS (*Breizh Synthesis System*) software platform for circuit design proposes a set of tools for the capture of application description (in VHDL or in C), the compilation, the simulation and the synthesis of architecture.

The platform is currently composed of the following modules.

- A set of programs (C and VHDL compilers, selection, scheduling, code generation) allowing the synthesis of circuits.
- Graphic interfaces, *PUDesigner and GFDesigner*, allowing the visualization and the handling of the data flow graphs and architectures.
- A tool for power estimation at the architectural level, *PowerCheck*, operating from the architectures generated by the synthesis. It also uses as an input a file of parameters which makes it possible to characterize the technology of the circuit and the physical capacities of the chips. The signal can be specified in two different ways: either by its probabilities according to a model (white noise, DBT), or in the form of a file of vectors from which are extracted the probabilistic characteristics. As output, PowerCheck provides a report indicating the average powers dissipated by each part of the control and processing units. PowerCheck also gives the dissipated powers cycle by cycle by the various modules.
- A tool for area and delay interconnection estimation, *Jfloorplanner*, operating at the architectural level. The input of the tool consists of a *netlist* generated by BSS. This netlist contains the whole of information related to the components and their interconnections. The tool provides indications concerning the final area of the floorplan, the length of the interconnections as well as the interconnection delays related to these lengths. A display of the estimated floorplan is available and can be used in order to carry out quickly the place and route step with standard CAO tools.

BOOST (Breizh Object Oriented Synthesis Tools) is an evolution of the BSS platform whose main objective is to facilitate the integration of new modules in the synthesis flow.

A global XML application defines the module list and the installation location. For each module, an XML application defines how the module has to be described to be included in the Boost platform. Several simple synthesis steps have been included in Boost. This platform was used as a demonstrator for the OSGAR project during the RNTL days in October 2004 in Rennes. Boost is developed in Java language and can be installed on solaris, windows or linux platforms.

To know some more, contact Daniel Chillet.

5.5. Gecos

Keywords: *Eclipse*, *Flexible Compilation*, *OSGi*.

Participant: Ludovic L'Hours [contact].

Gecos can be seen as an evolution of CALIFE (Vincent Messé and François Charot [7]) where a compilation flow is built from simple transformation tasks. In Gecos tasks are assembled using a simple script language: variables carry data (intermediate representation, profiling data, etc.) and functions call transformations. This simple language allows to easily create or customize compilation flows. Gecos is developed using OSGi plugins and Eclipse extension framework which ease the installation and the development of new transformation and analysis tasks. The platform is in active development but it already contains many transformations of a standard modern compiler (C frontend, SSA transformation, code selector, register allocator, etc.). It was successfully used as a base of a research project in custom instruction set generation.

Find more information on its dedicated web page *http://gecos.gforge.inria.fr*.

6. New Results

6.1. New architectures and technologies

Keywords: *CDMA*, *MVL*, *Network-on-Chip*, *NoC*, *SoC*, *System-on-Chip*, *computation grain*, *low-power consumption*, *multiple-valued logic*, *reconfigurable architecture*, *sensor network*.

6.1.1. New organization of reconfigurable structures

6.1.1.1. Memory hierarchy in specialized SoC

Participants: Daniel Chillet, Olivier Sentieys, Erwan Grace.

Our research aims at defining a global memory hierarchy model suited to SoC and a methodology which allows the designer to explore the design space. The main objective consists in limiting the energy consumption of the circuit.

SoC architectures already propose large on-chip memory, with several memory banks and memory hierarchical levels. In these systems, the main problem concerns the memory exploration in relation with the application needs and particularly the consumption problem of this part of circuit. Several problems could be addressed in this context, such as cache, scratch-pad, and multi-bank memory. We focus our research on designing methodologies for optimal memory hierarchies. A first model has been defined for dedicated SoC and for large reconfigurable architectures such as FPGA circuits. Another way to solve this problem is to extend the reconfigurable paradigm to the memory part. Recent ITRS[11] report indicates that static power consumption will grow significantly as transistor size shrinks. In order to limit it, we propose to alter dynamically the voltage of some area of the memory. We have demonstrated that this new concept, referred as virtual memory hierarchy, could result in significant consumption reduction [15]. At present, we investigate and evaluate different low power solutions for our future implementation. This work is done through a collaboration with the *Ecole Nationale Polytechnique d'Alger* (L. Abdelouel Ph.D.) and with the *CEA*.

6.1.1.2. ReMiX: Reconfigurable Memory for Indexing Huge Amount of Data

Participants: Gilles Georges [Symbiose], Steven Derrien.

Indexing is a well-known technique that accelerates searches within large volumes of data such as the ones needed by applications related to genomics, to content-based image or text retrieval.

The ReMiX project proposes the design of a dedicated and very large index memory (several hundred of Gigabytes, distributed among a cluster of nodes), big enough to entirely store huge indexes and avoid the use of any disk.

In addition, the index memory uses reconfigurable hardware resources to tailor – at the hardware level – the memory management for optimizing the support of the specific properties of the indexing schemes. It also offers the opportunity to implement parallel algorithms.

An hardware platform based on Flash memory technology has been developed by the R2D2 team. It comprises four RMeM node, each node being in the form of a standard PCI board. Each board integrates a high-end Xilinx Virtex-II FPGA coupled to 64 GBytes of Flash memory. The prototype is fully functional and several applications have already been ported on the architecture.

The strength of this approach is that this system combines the benefits of hard-drive storage (non-volatility, density), with those of memory (bandwidth, access time). In particular, large indexed databases, which usually suffer from prohibitive random access time when stored on a standard HDD, will largely benefit from an implementation on ReMIX (ReMIX random access latency is three order of magnitude lower than a commodity HDD).

This three-year project (October 2003 - September 2006), coordinated by the Symbiose project, was funded by the French ministry (ACI Data Mass program). The team R2D2 has been strongly involved in both the design of the hardware platform and the porting of a Content Based Image Retrieval application.

[11] http://www.itrs.net/Links/2005ITRS/Home2005.htm

6.1.2. Efficient Coding or Modulation Schemes for On-Chip Interconnection Networks

Participants: Sébastien Pillement, Olivier Sentieys.

We have worked on some new crosstalk[12] avoidance coding schemes for on-chip buses [29]. These schemes consist in encoding sequences of bits on each line of a bus transferring a packet in order to eliminate worst-case crosstalk patterns. They permit to improve the delay on the link at the cost of doubling the number of transmitted bits. The advantage of the presented solutions is that they have no wiring overhead, so they are independent from the bus bit-width. The coding schemes allow an increase of 50% of the data rate for a 1-mm bus. Moreover, the proposed solutions induce a direction in deep-submicron noise that can be used to implement a noise-tolerant system.

In [28], we introduced a new ternary link including a binary-to-ternary encoder and a ternary-to-binary decoder in voltage-mode multiple-valued logic (MVL). This link improves the transistor count compared to existing designs and it has no DC current path. The complete link was simulated with SPICE and a $0.13\mu m$ CMOS technology. It additionally shows interesting advantages on power consumption for global interconnects compared to full-swing signaling binary systems (up to 56.4% less energy consumption). Its low propagation delay is also an advantage in the design of high-speed on-chip links for asynchronous systems.

We have also introduced a new coding scheme that faces simultaneously different issues of interconnection design. It accelerates data transfer on a bus or on a network-on-chip by removing worst-case patterns that cause crosstalk issues. This is achieved by skewing odd and even signals on the link. The implementation of this system is very simple and area-efficient. It enables to improve bandwidth by a factor higher than 2.3 on a metal-2 UMC $0.13\mu m$ CMOS technology bus with the same number of wires than a shielded bus. Furthermore, the delay propagation is well-controlled since the solution that is used to face crosstalk phenomenon removes all transition patterns but two. It also greatly improves noise tolerance through the use of a combination of two error detecting codes at the expense of a reduced number of additional wires. The first code uses temporal redundancy and the second code is a parity-based scheme. This property enables us to lower the power supply voltage in order to reduce power consumption.

6.1.3. Wireless sensor networks

Participants: Olivier Berder, Mickaël Cartron, François Charot, Ludovic L'Hours, Patrice Quinton, Olivier Sentieys, Charles Wagner, Tuan-Duc Nguyen.

Wireless sensor networks in 2006 became an important domain of research activity for R2D2 because of the great potential of this technology in the future, and the difficult challenges that are posed by it.

Based on the prior activity and experience of Mickaël Cartron and Olivier Sentieys on energy efficiency for sensor nodes, R2D2 was at the initiative of an RNRT project, named SVP (for SurVeiller et Prévenir) together with several companies and teams: CEA LETI, Thales, INRIA, LPBEM, AphyCare, ANACT, Lip6 and Institut Maupertuis. This project aims at developing platforms for sensor network applications. One of these applications is the monitoring of children's physical activity. For this application, R2D2 will have the responsibility of developing the hardware and software infrastructure for the prototype application. This development will be based on the experience accumulated by Michaël Cartron on the prototype already developed in the team. Moreover, R2D2 is also involved in a region sponsored research project named CAPTIV where applications of sensor networks for automotive applications are studied.

Beyond these applications – which are per se interesting research, as few such experimental platforms exist – the aim of our research is to study the relationship between algorithms and energy efficiency in such distributed environments.

Mickaël Cartron presents in his thesis[12] results regarding the optimization of energy efficiency for low-level communications, by trying to find trade-offs between transmission power and error rate of the transmission. He has been able to show that an optimal tradeoff exist where 75% of the power can be saved as compared to the worst case transmission. This study could be the basis of hardware implementations of low-level communications, either using ASIC technology or reconfigurable hardware.

[12] A disturbance, caused by electromagnetic interference, along a circuit or a cable pair.

Optimization of energy efficiency will be a research subject in the SVP and CAPTIV projects. In SVP, the problem will be considered at the application level, in order to find out trade-offs between local memorisation and compression and transmission of data. In CAPTIV, the problem will be considered at the low-level transmission layer, by trying to use MIMO (Mutiple-Input Multiple-Output) systems to improve the energy efficiency of communications. In such a scheme, some nodes can cooperate at both the transmission and the reception sides in order to create a distributed MIMO system. By using cooperative MIMO transmission instead of SISO, it is shown that the distance between nodes can be increased and a large amount of the total energy can be saved for middle and long distance transmission. Considering Alamouti and Tarokh space-time block codes (STBC), we proposed an optimal selection of the number of antennas at both the transmission and the reception sides with respect to the transmission distance. The energy efficiency of cooperative MIMO over SISO and multi-hop SISO was proved by simulations, and we proposed a multi-hop technique for cooperative MIMO that represents a very interesting compromise for a limited number of available cooperative nodes.

Notice that all this research activity is pushed by the strong links of R2D2 with the Aphycare[13] company, a spin-off of the R2D2 team, whose activity aims at developing wireless sensors nodes for the care of elder persons.

6.1.4. Multiple-Valued Logic (MVL) architectures and circuits

Participants: Daniel Chillet, Ekué Kinvi-Boh, Olivier Sentieys.

In this work, we focus on the design of new architectures based on the principle of Multiple Valued Logic (MVL). The potential advantages of such architectures can allow a reduction of the number of interconnections in the chip and a reduced packaging. The focused aim is thus to validate by testing fabricated ternary circuits, new concepts known as SUS-LOC (SUpplementary Symmetrical LOgic Circuit) which allow the design of circuits in ternary logic and which are based on the use of depletion and enhanced mode MOSFET transistors. For that, the set up of a methodology and design tools suitable for ternary logic and SUS-LOC concepts, is necessary. This research work articulates around three principal points, developed in the thesis of Ekué Kinvi-Boh [13].

The first aspect of our work consisted on designing and characterizing SUS-LOC circuits. A characterization flow allowing to extract the circuit performances such as delay and the energy consumption due to transitions was developed. An experimental library of models of transistors enabled us to quickly define a design methodology based on the method of the switches. Although more complex, the SUS-LOC circuits have delay performance and average energy consumption close to those of their binary equivalents.

The second aspect relates to the modeling and estimation of performance of SUS-LOC circuits. Thus, an estimate flow of performance starting from models of the design circuits described in VHDL language was developed. The data on delay and energy consumption obtained from the characterization of the basic structures of the modelled circuit is integrated in this flow. In the same way, it was developed a VHDL package dedicated to ternary logic. The estimated performance by this flow is the total energy consumed by a circuit over a given duration.

The last aspect of this research relates to the fabrication of integrated circuits, including a four TRITs (TeRnary digITs) adder and a 64 cells ternary SRAM memory. The fabrication flow is based on a ternary design-kit developed in collaboration with the UCL in Louvain-la-Neuve. The SUS-LOC circuits fabricated in SOI 2 μm technology required the addition of new masks to the fabrication process. Static and dynamic tests were carried out on fabricated SUS-LOC chips.

6.2. Modeling, synthesis and compilation for reconfigurable platforms

Keywords: *architecture modeling ASIP design*, *architecture synthesis*, *communication*, *fixed-point arithmetic*, *flexible compilation*, *reconfigurable system*, *scheduler*, *synthesis*, *system on-chip*.

[13] http://www.aphycare.com/

6.2.1. Synthesis and compilation techniques

6.2.1.1. Derivation of efficient architectures for regular arrays

Participants: Steven Derrien, François Charot, Alain Darte [CompSys INRIA Rhône-Alpes], Tanguy Risset [CompSys INRIA Rhône-Alpes], Anne-Marie Chana, Patrice Quinton, Christophe Wolinski.

Our research aims at developing methods and tools to synthesize parallel architectures for data-intensive applications expressed using the Alpha applicative language. These methods are implemented in the MMAlpha software.

The Alpha language allows systems to be modelled using structured descriptions: some components can be separately represented, and later instantiated as an elementary block in a larger application. In many applications, these blocks have different clock rates, and it is the case for example, in the WCDMA (Wireless Code Division Multiple Access) air interface. We have been able to represent in Alpha multi-rate systems, by adding special components that model up- and down-samplers, and we have extended the structured scheduler of MMAlpha in order to find out the rates of all elementary blocks as well as the detailed schedule of each block. This activity, which was started during the thesis of Madeleine Nyamsi in 2005, is being pursued in the frame of a research co-operation with the Laval University in Québec city and UQTR (Québec) for the modelling of MIMO communication schemes.

Another research avenue is to relate the polyhedral model – the theoretical model of Mathematica – to other important models for architecture specification and synthesis. This work is done in cooperation with the Espresso project-team of IRISA. The context is the design of integrated circuits for multimedia applications using jointly the data-flow model, the polyhedral model, and high-level synthesis methods. The objective is to take benefit of these models in order to optimize systems containing both control aspects and intensive computations. The study relies on three modeling platforms : Polychrony with Signal, MMAlpha with Alpha and Gaut for high-level synthesis.

Generating automatically *efficient* interfaces between the kind of accelerators that regular array synthesis produced and the rest of the SoC where this element is introduced is often the most tedious and error-prone part of a design and it has often a strong influence on the actual performance benefits provided by the hardware acceleration. To solve this problem, we proposed to formulate it as a classical resource-constrained program, and thanks to recent optimization techniques [38], we were able to define conditions for obtaining a conflict-free schedule of input/output for multi-dimensional processor arrays (e.g., 2D grids) [37]. Since the schedule is static, it allows us to perform further optimizations such as grouping successive data in packets to operate in burst mode. A comparative approach (targeting FPGA technology) between our static schedule and a run-time congestion resolution has shown important gains in hardware area, while preserving the design clock period. We are currently working on an extension of our hardware interface model that would take advantage of this static I/O schedule to allow data prefetching and buffered write techniques, combined with a custom scratch-pad memory.

6.2.1.2. Automatic synthesis of optimized reconfigurable systems

Participant: Christophe Wolinski.

This year we have continued investigating the problem of optimized Fabric synthesis[14].

In this context we have studied how to bind the application data flow graph to the run-time reconfigurable heterogeneous Fabric cells in order to increase the performance of the entire system.

The binding and scheduling problems were defined and solved using a constraints-programming approach. This approach made it possible to obtain optimal solutions in terms of execution time while the number of run-time reconfigurations is minimized. As a result of our research, an automatic tool was developed.

6.2.1.3. Specialized microcontroller synthesis on FPGA

Participant: Ludovic L'Hours.

[14] This work is an extension of research on an automatic optimized reconfigurable system synthesis undertaken at Los Alamos National Laboratory, USA.

This research aims at developing techniques to synthesize specialized microcontrollers on FPGA. The targeted applications are described in a high-level language such as C, where control strongly prevails (peripheral control driver, packet processing, etc), such as the operating system embedded into the RDisk machine [45]. The main goal is to get small-sized circuits, with reasonable performances. The traditional approaches of architecture synthesis generally aim at maximizing the performance by analyzing and paralleling the data flow, there are not suited to applications with complex control flow. Their intrinsic sequential feature naturally leads to use software compilation techniques.

We designed a microcontroller synthesis technique based on the extraction of a specialized instruction set from a given application. The design of this instruction set is mainly leaded by application profiling information, but also by different estimators such as the pattern complexity or the number of bus access. The microcontroller is then derived from this instruction set using VHDL templates: the targeted architecture is currently a RISC processor, but other kind of architectures such as VLIW could be considered. Compared to fixed instructions set microprocessors, we managed to reduce by a magnitude of 2, both the code size and the processor size, for the same range of performances [52].

All these algorithms where integrated in a generic compilation platform called Gecos. This platform in constant development is freely available (http://gecos.gforge.inria.fr). Investigation are currently undertaken to use this methodology to generate processors for very constrained devices, such as nodes of a sensor network.

6.2.1.4. Architecture description language

Participants: François Charot, Julien Lallet, Sébastien Pillement, Olivier Sentieys.

Our research aims at developing methods to model programmable processors through their instruction sets and tools to derive software development environments from these processor models. A processor description in ARMOR is a grammar whose each derivation is a possible behavior of the instruction set. ARMOR thus describes the behavior of the instruction set, including its semantics, temporal information, the use of the resources, as well as the possibilities of parallelism at the instruction level.

The future objective is to extend this work for the modelling of reconfigurable and specialized SoC architectures with the goal to exploit such models in retargetable compilation flows adapted to reconfigurable architectures. A new study concerning the definition of a platform-based reconfigurable architecture has started. The main goal is to define a generic architecture (based on the DART paradigm) supporting different applications domains. The study has begun with the definition of a very flexible network. This network is able to connect and to enable communication between every kind of dynamically reconfigurable heterogeneous resources. The definition of the architecture is done with the help of a high-level architecture description language based on the MAML language developed at the University of Erlangen-Nuremberg. We developed a tool able to analyse the description and to produce an adequately synthesisable VHDL model. This generated network is associated with a flexible reconfiguration process which is not depending on the type and the quantity of the hardware resources. Due to local memories and a separated configuration path, the reconfiguration process is executed in one clock signal. Currently, some experiences are done concerning the implementation of preemptive resources.

6.2.2. Floating-point to fixed point transformation

6.2.2.1. Floating-point to fixed-point conversion methodology for FPGA

Participants: Daniel Menard, Nicolas Hervé, Daniel Chillet, Romuald Rocher, Olivier Sentieys.

A new methodology to implement floating-point applications into an FPGA using fixed-point arithmetic is proposed. The user has to specify the application time and accuracy constraint (expressed as the minimum output Signal to Quantization Noise Ratio). Then the methodology converts the application into fixed-point. Our approach aim is to determine the fixed-point specification which minimizes the architecture cost and leads to a sufficient computation accuracy expressed through the accuracy constraint.

The fixed-point conversion process must determine, for all data, a word-length and a binary-point position. It is composed of three main tasks. The first step corresponds to the data dynamic range evaluation. These results are used in the second step to determine the binary point locations. The third step objective is to fix the data word-length, such that the architecture cost is minimized and the accuracy constraint is satisfied. The accuracy is evaluated with an analytical method to reduce dramatically the optimization time compared to simulation based methods. To generate an optimized architecture, the operator word-length optimization and the synthesis process are coupled [17]. Thus, an iterative process on high-level synthesis and operator word-length optimization is used to improve both of these dependent processes. This coupling allows reducing the architecture operator number. Indeed, smaller word-length operators have a reduced latency. Compared to classical implementations based on a uniform word-length, our approach reduces architecture cost from 20 % to 40 % [18], [33].

6.2.2.2. Fixed-point accuracy evaluation

Participants: Daniel Menard, Romuald Rocher, Pascal Scalart, Olivier Sentieys.

An important part of the floating-point to fixed-point process is the fixed-point accuracy evaluation. The accuracy is evaluated through the Signal to Quantization Noise Ratio (SQNR). A general method based on an analytical approach has been proposed. This method is valid for all quantization laws (truncation and rounding) and for all systems including arithmetic operations. The proposed technique is based on a matrix model which simplifies the expression for transform algorithms such as FFT or DCT. For recursive systems, the method unrolls the recurrence. The complexity of our approach has been determined. To reduce this complexity, a linear prediction model has been developed. This model accelerates recurrence unrolling by approximating the recurrence terms included in the output quantization noise analytical expression. The model has been evaluated and compared in terms of accuracy and computing time for different applications such as, Least Mean Square (LMS) or Affine Projection Algorithms (APA). This approach leads to accurate noise power estimations. Model execution times have been evaluated on the Matlab tool. The linear prediction approach reduces dramatically the noise power expression computing time.

The output noise analytical expression is used in the floating-point to fixed-point conversion process to optimize the data word-length under accuracy constraint (SQNR minimal value). The optimization time obtained with our approach is better than that obtained with fixed-point simulation based approach after only several iterations. Our approach reduces computing time compared to simulation approaches after only some iterations. These results show the interest of our methodology to reduce fixed-point system development time. They are described in details in the Ph.D. thesis of Romuald Rocher[14].

A method has been proposed to define the accuracy constraint (SQNR minimal value) according to the application performance constraints. The SQNR minimal is obtained with a floating-point simulation. The error due to the fixed-point conversion is modelled by a single noise source located at the system output. This noise source power is increased as long as the application performances are not modified. The noise model has been defined and validated through different experiments. Our approach to determine the accuracy constraint has been tested and validated on two applications corresponding to a MP3 coder and a WCDMA receiver.

6.2.3. Specialized SoC architecture modeling

6.2.3.1. System modelling for dynamically reconfigurable architectures

Participants: Imène Benkermi, Didier Demigny, Daniel Chillet, Sébastien Pillement, Olivier Sentieys.

SoC platforms including dynamically reconfigurable units aim at supporting complex multimedia applications using a real-time operating system. They consist in different execution modules, i.e. general-purpose processor(s) and specialized/reconfigurable accelerators including the DART dynamically reconfigurable architecture. Their heterogeneity led to a specification by means of the three following levels of description: software, middleware and hardware. Each level corresponds to a task configuration on the platform. Hence, the operating system has to ensure specific services imposed by the reconfigurable aspect; namely, ensuring task communication and migration between the three levels of description.

The software model describes the different tasks of the application supported by the architecture platform. A UML-based model has been used. In addition to the task characteristics, real-time constraints and links between tasks, this model permits to specify the different forms a task can have depending on the target it will eventually execute on. This work has been done through a collaboration with ETIS (Cergy-Pontoise) and LESTER (Lorient) laboratories and it will continue through the OverSoC ANR project.

Another important issue for dynamically reconfigurable SoC platforms is the scheduling and binding of tasks on a heterogeneous architecture, eventually at run-time. We have proposed an approximate on-line scheduling algorithm based on Artificial Neural Networks (ANN), and more precisely on the Hopfield model. This scheduler is able to distribute the task set on different computing units, while meeting their real-time constraints and taking into account their heterogeneity; i.e. one task may have different execution times depending on the unit it will execute on. To take into account all of the constraints, we introduce a new design rule to built the neural network. A mathematical formulation of this new design rule has been done and a simulation tool has been developed. We have shown that correct schedule can be obtained with a small number of iterations. We will then study a hardware implementation of the neural network on a reconfigurable structure to obtain an efficient and reactive on-line scheduling.

6.2.3.2. SoC modeling and prototyping on FPGA-based systems

Participant: François Charot.

R2D2 participates in the SocLib initiative (http://soclib.lip6.fr), whose goal is to build an open platform for modeling and simulation of multi-processors system on chip. The core of the platform is a library of simulation models for virtual components (IP cores), with a guaranteed path to silicon.

Thanks to the increasing capacity of FPGA components, it is today possible to integrate a significant number of processors in a programmable FPGA component. Although it is possible to synthesize a processor core in such a component, the FPGA manufacturers design their own processor architectures. As an example, Altera propose the Nios processor core, declined in three families (economic, standard, fast). It is configurable processor core (pipeline depth, cache size, custom instructions, etc.).

As part of our participation to this initiative, we study the feasibility of prototyping SocLib platforms using FPGA components. A cycle-accurate and bit-accurate (CABA) model of the Nios processor core from Altera has been designed. In the near future, it will be integrated in the SocLib platform which will be developed in an ANR RNTL project. This work is done with the goal to establish a link between a SocLib simulation platform and its prototyping on a FPGA system.

6.3. Study of applications

Keywords: *WCDMA*, *biomedical*, *image indexing*, *intrusion detection in hardware*, *mobile telecommunication*, *speech processing*.

Applications stemming from third-generation radio-communication systems are good candidates for the study of hardware systems mixing programmable parts executing software code and specialized modules dedicated to the acceleration of time consuming parts of applications.

Data filtering, cryptographic and traffic filtering in high-speed network, speech processing are also under consideration.

6.3.1. Radio-communication systems

6.3.1.1. Mobile communication systems prototyping (3G, MIMO)

Participants: François Charot, Olivier Berder, Michel Guitton, Daniel Menard, Patrice Quinton, Taofik Saïdi, Pascal Scalart, Olivier Sentieys, Charles Wagner.

Our experiments rely on the use of the SignalMaster prototyping platform[15] that allows applications described using Simulink to be executed on a special-purpose board including a DSP processor and a FPGA chip (SignalMaster platform from Lyrtech Inc. company). Different implementations of the WCDMA emitter-receiver have been realized. This research is a preliminary step in the study of fast estimation techniques for the design of SoC and is described in full details in the Ph.D. thesis of Madeleine Nyamsi in 2005. Arithmetic aspects have been studied for the WCDMA receiver implementation. The aim is to find the fixed-point specification which maintains the application performances and minimizes the operator word-length. This specification is obtained with our approach for floating-point to fixed-point conversion. The real performances are measured through fixed-point simulations.

In the context of wireless communications, using more than one antenna both at the transmitter and at the receiver optimizes the spectral efficiency data transmission. The high complexity of the MIMO (Multiple Input Multiple Output) and multi-antenna algorithms leads to the design of real-time high-performance specific architectures. A flexible MIMO real-time prototype has been designed to operate under the WCDMA (Wideband Code Division Multiple Access) third generation cellular standard. It can be used for uplink (HSUPA) and downlink (HSDPA) communications. The circuit is characterized by a scalable and flexible parallel-pipeline architecture. This system is designed on a rapid prototyping platforms from Lyrtech Inc. company, the SignalMaster platforms, for real-time measurements. This work is done in collaboration with Lyrtech Inc. and with the LRTS laboratory of Laval University in Québec, CA.

6.3.1.2. Parallel reconfigurable architectures for LDPC decoding

Participants: François Charot, Christophe Wolinski.

LDPC codes are a class of error-correcting code introduced by Gallager [41] with an iterative probability-based decoding algorithm. Their performances combined with their relatively simple decoding algorithm make these codes very attractive for the next satellite and radio digital transmission system generations. LDPC codes were chosen in DVB-S2, 802.11n, 802.16e and 802.3an standards.

The decoding of LDPC codes is an iterative process. For 802.16e standard about 3 000 messages are processed and reordered in each of the 30 iterations. The amount of messages is much more higher in the case of DVB-S2 (of the order of 300 000 messages). These huge data processing and storage requirements are a real challenge for the decoder hardware realization, which has to fulfill a specified throughput (30 Mbit/s for 802.16e and 255 Mbit/s for base station applications in case of DVB-S2).

One major problem is the huge design space composed of many interrelated parameters which enforces drastic design trade-offs. An other important issue is the need for flexibility of the hardware solutions. The aim of our research which is carried out in collaboration with the R-Interface company is the definition of a generic architecture template adapted to the 802.16e standard. The definition of the architecture is based on the use of optimization tools able to schedule the computation and the memory accesses of the algorithm. In order to validate the architecture template, a performance estimation model written in SystemC of the proposed generic architecture is being developed.

6.3.2. Image and multimedia processing

Participants: François Charot, Charles Wagner, Christophe Wolinski.

Image and video processing have been significant application drivers for the reconfigurable computing community since the early 1990's. Reconfigurable computers have been used most widely, and successfully, for accelerating low-level image processing algorithms like local neighborhood functions. These functions are also called sliding window functions or spatial filters, and are used extensively in image processing and computer vision. Local neighborhood functions are applied at a particular pixel location and their output depends on a finite spatial neighborhood. The function is applied independently at all pixel locations and is typically constant across all pixel locations.

[15] http://www.lyrtech.com/DSP-development/dsp_fpga/signalmaster.php

Our research concerns the study of a parametric run-time reconfigurable architecture model for local neighborhood image processing. The proposed architecture model is an example of a polymorphous fabric [11] that consists of simple, inter-connected cells, each with an optional local memory. In general, the cells composing the fabric may contain different groups of homogeneous cells. Each cell's data-path may have its own controller, or alternatively, a group of identical cells may share a single controller. A single controller can control one or more cells, to perform computations, to read/write local memory, to synchronize with the processor, and to communicate with other cells. Cells require only local connections and there is very little overhead in terms of resource utilization. In some cases, it is possible to use 96% of the FPGA hardware resources. The Fabric (size of the fabric, number of levels, size of the image, buses and data-paths, etc. are parametric) is composed of optimized generic cells that have two important properties. The first is that they contain the sliding window modules that operate over a partial image stored in local memory. Access to the data inside the sliding window is transparent to the user (that means that the user always addresses the particular pixels relative to the sliding window). The second property is that the different functions such as convolution, minimum, median etc. can be translated into software micro-code for the cells programmable controller if a multi functional data-path is assembled in which case run-time reconfiguration is possible. The developer can select the number and type of functions and connect them to generate a more complex algorithm.

Experimental results [30], [31] show that for a satellite image feature extraction application, the architecture, implemented on Stratix II and Virtex 2 Field Programmable Gate Arrays, achieves similar performance, hardware resource utilization, and throughput as a fully pipelined systolic array architecture, yet offers improved flexibility to the developer.

6.3.3. Content-based image retrieval hardware acceleration

Participants: Steven Derrien, Auguste Noumsi, Patrice Quinton, Laurent Amsaleg [Texmex].

Content Based Image Retrieval (CBIR) is a technique that allows one to retrieve images of a data base which are (at least) partly similar to a given reference image. CBIR is drawing increasing interest due to its potential application to problems such as image copyright enforcement. Indeed, the large use of Internet resulted in a huge increase of Web available multimedia content, especially images. Checking copyright is therefore a concern for image owners which must be able to identify undue use of images. This identification process relies upon precise and fast image comparison algorithms as Internet is a rapidly changing support and such algorithms need to be run on a daily basis.

Although accurate search techniques based on local image descriptors exist, they suffer from very long execution time (retrieving an image among a 30,000 image data base requires about 1,500 seconds on a standard workstation). To make these techniques attractive, we have been working on the acceleration of CBIR through the use of specific hardware design architectures, the target machines being the RDISK cluster [27] and the ReMIX machine [25].

Among other results, we have extended the results obtained in 2005, by showing that the encoding of the image descriptors (initially in single precision floating point) could be reduced, through a non-linear transformation, to 3 bits encoding while preserving the search accuracy. Although this analysis was initially done in the context of an hardware implementation, it is to note that this result is also of interest to the image processing community, since it allows descriptors database size to be reduced by a factor of 10.

6.3.4. Intrusion detection system in hardware

Participants: Georges Adouko, François Charot, Christophe Wolinski.

The dynamic feature of security systems is – through anti-intrusion mechanisms (filtering at different levels: packet, connection, and application levels) evolving according to modes and levels of protection–, to our knowledge, a challenge out of reach of classical technologies based on general purpose or network processors. The requirements of security in high-speed networks (from 10 to 40 Gigabit/s) impose the implementation of the filtering rules in the appropriate hardware structures. It is a matter of being able to manage a large variety of complex treatments, and also to guarantee the quality of service. Only dedicated solutions could solve the bottleneck related to the implementation complexity today, at the price of an obvious lack of flexibility and a total absence of evolution.

The aim of our research (Fastnet PRIR Project) is the design of specialized hardware systems for filtering of the network traffic at high-speed. Even if the work especially concerns the study of efficient and predictable filtering techniques and their implementation on FPGA programmable components, our approach rests on a system view of the intrusion detection system and envisions specialized systems combining software and hardware modules. Different approaches to the pattern search problem used for filtering the traffic have been carefully studied and compared from the point of view of the amount of hardware resources, the expressiveness of regular expressions, the throughput and the number of patterns [20].

6.3.5. Accelerating Statistical Test for Real-Time Estimation of Randomness

Participants: Renaud Santoro, Olivier Sentieys.

Many applications need high-quality random numbers. In cryptography, most of the secured systems are based on unpredictability of a single key, and therefore on the quality of the original random seed. Statistical theory is used to determine the randomness of a stream of numbers. Statistical tests have been developed in literature, and test batteries like Diehard, Nist and FIPS 140-2 are now recognized as a reference. If the random number generator (RNG) passes a number of qualitative statistical tests for randomness, the RNG is considered to be random with some degrees of confidence. However, this procedure is slow and statistical tests are applied on only few bytes. In the case of true random number generators, random sources can vary in time, and the statistical tests must be able to check the RNG quality continuously in real time. During this year, we have investigated the acceleration of some statistical tests in hardware to enhance their efficiency and to detect RNG failures. We have measured the performance and the cost of hardware implementations into FPGA or VLSI, for FIPS 140-2 test suite, autocorrelation and entropy tests. Results show that the system can be used at high-rate for obtaining higher quality random sources.

6.3.6. Intelligent transport system (ITS)

Participants: Olivier Berder, Daniel Ménard, Olivier Sentieys, Tuan-Duc Nguyen.

Transportation systems are playing a critical role in virtually all facets of modern life and significant challenges remain to further improve the efficiency and safety of the current systems. The Brittany Region Council and the Côtes d'Armor Department Council are actually investing in this research area and created recently a Scientific Interest Group on Intelligent Transportation System (ITS), whose head is at ENSSAT, Lannion. Our research team actively participates to this new activity, and especially to projects concerning the deployment of new energy-efficient architectures for ITS.

R2D2 is the leader of the regional research program CAPTIV, which aims at proposing new low-cost and energy-efficient mobile communications solutions to ease and make safer road traffic conditions. Considering "intelligent" road signs and vehicles, i.e. equipped with an autonomous radio communication system, drivers will be able to receive at any time various information about traffic fluidity or road sign identification. In order to reduce deployment cost and increase lifetime of the whole system, Multi-Input Multi-Output (MIMO) signal processing techniques are used. Such techniques allow to dramatically increase the capacity of mobile communication systems or the quality of the transmission, thanks to the well known space-time codes. From another point of view, MIMO systems allow to significantly reduce energy consumed by communications in ad-hoc networks. Considering each crossroads as a communication node, the possible cooperation between road signs allows energy-efficient communications between crossroads. Supported by the Scientific Interest Group GIS ITS-Bretagne and by industrial leaders in ITS domain, regrouping major research laboratories in the region, CAPTIV is a highly applicative program. A first prototype of such a communicating crossroads will be presented in the *R*oute du Futur in Saint-Brieuc (portion of road devoted to ITS experimentations).

7. Contracts and Grants with Industry

7.1. Specialized architecture for decoding LDPC codes (2006)

Participants: François Charot, Christophe Wolinski.

The work is granted by R-interface[16], a technology and wireless IP provider for baseband communication systems. The work concerns the study of parallel and generic architectures adapted to the 802.16e standard.

7.2. ANR RNRT SVP (2006-2008)

Participants: Olivier Berder, Mickaël Cartron, François Charot, Ludovic L'Hours, Olivier Sentieys, Patrice Quinton, Charles Wagner.

The main goal of the ANR SVP (http://svp.irisa.fr), (*SurVeiller et Prévenir*) project is to study, to experiment and to realize an ambient integrated architectural framework dedicated to the design and to the deployment of services into a dynamic sensor network. The proposed framework will consist in designing a system architecture that will meet the objective of ease of use or convenience while also taking into account and adapting all specific characteristics of wireless sensor nodes like drastic resource constraints. Since we are convinced that only technologies are not enough to spread and promote advanced researches we insist on the societal aspects of the project by also taking into account the final user. The second main objective of the SVP project is to deploy real applications in situ in order to adapt the technology available on the shelf to the reality. The first application will consist in deploying a sensor network that will record the physical activity of school children in order to study and prevent childhood obesity. In the second application, a sensor network will be deployed in an harbor area in order to warn workers when risk of accident may arise and to help in localizing and optimizing the containers management.

7.3. Contract with Thomson (2006-2009)

Participants: François Charot, Christophe Wolinski.

The Ph.D. thesis of E. Raffin is supported by a CIFRE grant in the framework of a contract between R2D2 and Thomson.

8. Other Grants and Activities

8.1. Regional Actions

8.1.1. Fastnet: Fast Adaptative Secure Technology for high-speed NETwork (2005-2007)

Participants: Georges Adouko, François Charot.

The Fastnet project has been contracted in March 2005, It is granted by the Brittany Region and it involves ENST Bretagne. It tackles the problematic of high-rate filtering, using architectures based on reconfigurable components that allow at the hardware level, specific filtering algorithms to be implemented, and exhibiting this way a high degree of parallelism.

8.1.2. CAPTIV (2006-2008)

Participants: Olivier Berder, Tuan Duc Nguyen, Olivier Sentieys.

The CAPTIV project has been contracted in January 2006. It is granted by the Brittany Region and it involves ENST Bretagne and IETR laboratories. The scientific objective of this research program is the study and the realization of communication systems between vehicles and road infrastructure (e.g. signs traffic) at low cost and at low-energy consumption .

8.1.3. PucesCom-Santé (2006-2008)

Participants: François Charot, Patrice Quinton, Olivier Sentieys, Charles Wagner.

[16] http://www.r-interface.com

The PucesCom-Santé project has been contracted in January 2006, It is granted by the Brittany Region. PucesCom-santé is managed by the Brittany branch of the ENS de Cachan and it involves several laboratories of the Brittany region: LPBEM (Rennes 2), IRISA, IETR and LTSI. The project concerns the use of a biometric data sensor network for the follow-up of the physical activity and energy expenditure of a population

8.2. National Actions

The team R2D2 participates to the activities of:

- GdR SOC-SIP (*System On Chip - System In Package*).
- GdR-PRC ISIS (*Information Signal ImageS*), working group GT7 *Algorithms Architectures Adequation*.
- GdR ASR (*Architectures Systèmes et Réseaux*), R2D2 is a member of the group *RECAP*[17] group.

8.2.1. ReMiX: Reconfigurable Memory for Indexing Huge Amount of Data (2003-2006)

Participants: Gilles Georges [Symbiose], Steven Derrien.

Indexing is a well-known technique that accelerates searches within large volumes of data such as the ones needed by applications related to genomics, to content-based image or text retrieval.

The ReMiX project proposes the design of a dedicated and very large index memory (several hundred of Gigabytes, distributed among a cluster of nodes), big enough to entirely store huge indexes and avoid the use of any disk.

In addition, the index memory uses reconfigurable hardware resources to tailor – at the hardware level – the memory management to best support the specific properties of the indexing schemes. It also offers the opportunity to implement algorithms having potential parallelism.

An hardware platform based on Flash memory technology is being developed by the R2D2 team. The platform consists of several computing nodes connected through a high performance network interface. Each node is based on a Xilinx FPGA processing element coupled to 64 Gbyte of Flash memory. This approach allows to combine the benefits of hard-drive storage (non-volatility, density), with those of memory (bandwidth, access time) to efficiently support large indexed databases.

This three-year project (October 2003 - September 2006), coordinated by the Symbiose project, is funded by the French ministry (ACI Data Mass program). The team R2D2 is strongly involved in the design of the hardware platform.

8.2.2. OverSoc (2005-2008)

Participants: Daniel Chillet, Sébastien Pillement.

OveRSoC is an ANR project which has been contracted in december 2005 for 3 years. The project objective is to develop such global exploration methodology to evaluate and validate the interactions between an embedded RTOS and a Reconfigurable SoC (RSoc) platform. The OveRSoC project aims also at furnishing SoC designers with a framework for choosing the right RTOS services architecture according to a particular reconfigurable SoC platform. This project involves Architecture team of Etis (UMR 8051) and the Lisif laboratory (EA 2385).

8.3. International bilateral relations

8.3.1. Europe

8.3.1.1. Comap project: collaboration with Germany

Participants: Julien Lallet, Sébastien Pillement, Olivier Sentieys.

[17] http://www2.lifl.fr/sensor/

The CoMap project (https://comap.enstb.org/) deals with the systematic mapping, evaluation, and exploration of massively parallel processor architectures that are designed for special purpose applications in the world of embedded computers.

This is a French-German project with several teams from the both countries:

- Hardware-Software-Co-Design, Department of Computer Science, University of Erlangen-Nuremberg
- Laboratory of Circuits and Systems, Department of Electrical Engineering and Information Technology, Dresden University of Technology
- Architecture and Systems, LESTER, Université de Bretagne Occidentale
- R2D2 research team from IRISA, Université de Rennes
- High Performance Computing and Architecture, ENST Bretagne

The investigated class of computer architectures can be described by massively parallel networked processing elements that, using today's hardware technology, may be implemented on a single chip (SoC - System on a Chip).

8.3.1.2. Other european collaboration

R2D2 cooperates with the University of Leiden in the Netherlands (Ed Deprettere) on parallel architecture synthesis.

R2D2 cooperates with UCL at Louvain-La-Neuve on the topic of ternary technology integrated circuits. A prototype circuit has been developed with the SOI technology of the micro-electronics laboratory (DICE of UCL).

R2D2 cooperates with Lund University (Sweden) on Constraints Programming approach application in the reconfigurable data-paths synthesis flow.

R2D2 cooperates with the university of Girona in Spain (Computer Vision and Robotic Group of the Institute for Informatics and Applications) on parallel architectures for vision algorithms applied to underwater robot.

8.3.2. Africa

R2D2 cooperates with ENIT in Tunis on the topic of mobile telecommunication architectures.

R2D2 cooperates with the university of Antanarivo and the Polytechnic Superior School of Antananarivo in Madagascar, for the training of faculty members.

8.3.3. North America

R2D2 maintains relations with the computer science department of the University of Colorado State in Fort-Collins on the development of MMAlpha.

R2D2 cooperates with the LSSI laboratory of Trois-Rivières university in Québec, on the design of architectures for filters.

R2D2 cooperates with Los Alamos National Laboratory (USA) on optimized reconfigurable architectures implementations for low-level image processing.

R2D2 cooperates with the University of California, Riverside, on optimized image processing applications synthesis.

R2D2 cooperates with the LRTS laboratory of Laval university in Québec on the topic of architectures for MIMO systems.

8.4. Visiting scientists

- Adam Postula (University of Queensland, Australia) from 09/11/06 for 2 months.
- Sébastien Roy (Laval University, Canada) from 06/21/06 for 2 weeks.
- Simon Savary, Michel Thériaul (Laval University, Canada) from 11/1/06 for 1 month.

9. Dissemination

9.1. Activities in the scientific community

O. Sentieys is a steering committee member of the SOC-SIP Expert Group at the department STIC of the CNRS. He is the chair of the IEEE Circuits and Systems (CAS) french chapter. He is a member of the French National University Council since 2000 in signal processing and electronics (Conseil National des Universités en 61ème section). He was a member of technical committee of the following conferences: DDECS, ISQED, DCIS, VTC, SYMPA, GRETSI, JFAA.

P. Quinton is member of the steering committee of the System Architecture MOdelling and Simulation (SAMOS) workshop.

P. Scalart is the head of electronics engineering department at Enssat.

C. Wolinski was co-organizer of "System Level Design, Methodologies and Tools" session at IEEE ISQED 2005 and of Workschop TCHA in conjunction with PACT 2006. He was a member of technical committee of the following conferences: DAC-2006, DATE 2006, DSD-2006, IQSD-2006, SYMPA-2006 and TCHA-2006. He was a member of Board of Directors of Euromicro Society.

F. Charot, S. Derrien, P. Quinton, C. Wagner and C. Wolinski participated to the scientific day organised in Rennes by the IETR laboratory on the topics: *Image et Systèmes embarqués* (January 2006).

9.2. Teaching and responsabilities

O. Berder teaches a course on *processors architectures* and signal processing at Enssat.

D. Chillet teaches a course on *advanced processors architectures* in Master STIR.

H. Dubois is the associate academic director at Enssat.

M. Guitton is in charge of the communication at Enssat.

L. Perraudeau is responsible for a course on the object languages in the DESS Isa (Computer science and its applications) of the university of Rennes 1, teaches the design of integrated circuits in DIIC second year), and teaches in Licence d'informatique, in Deug Sciences, mention SM and STPI.

P. Quinton is responsible for the parallel algorithmic course (Alpa module) in the Master in computer science of the university of Rennes 1, teaches in Deug Sciences, mention SM and STPI, and in DIIC (second and third year). P. Quinton is deputy-director of Ecole Normale Supérieure de Cachan, responsible of the Brittany branch of this school.

O. Sentieys is responsible for a signal and architecture module of the Master STI of the University of Rennes 1 and the DRT in electronic of Enssat. He teaches at Enssat and gives courses on *Methodologies for integrated system design* in Master STI and on *Low-power digital CMOS circuits* at Enst de Bretagne.

C.Wolinski is responsible for Computer Organization and Architecture branch in DIIC. He is responsible for the following courses: CSE "Design of Embedded Systems" (DIIC), SIA "Signal, Image, Architectures" (DIIC), XAA" Advanced Architectures" (ENSC).

Graduate student intern: Jean-Baka Domelevo, Sylvain Crétaux, Chikhi Rayan (Ifsic, France), Kevin Martin (ETGL, France).

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