INSTITUT NATIONAL DE RECHERCHE EN INFORMATIQUE ET EN AUTOMATIQUE

Project-Team DaRT

Dataparallelism for Real-Time

Lille - Nord Europe

Theme : Embedded and Real Time Systems

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DaRT is a common project with the University of Science and Technologies of Lille (USTL), via the Laboratory of Fundamental Computer Science of Lille (LIFL, associated to the CNRS as UMR 8022).

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2. Overall Objectives

2.1. Introduction

For the last few years we have seen the beginning of the "design gap". This gap is caused by the exponential growth of the integration rate of transistors on chips and the comparatively slower growth of the productivity of the integrated circuits designers. It is now impractical to fill a chip with custom designed logic. One has to reuse existing design parts or fill the chip area with memory (a good example of this evolution is the multi-core processors that include several existing processing cores instead of complexifying a single core). This evolution is clearly attested by the International Technology Roadmap on semiconductors.

In the same time, the computing power requirements of intensive signal processing applications such as video processing, voice recognition, telecommunications, radar or sonar are steadily increasing (several hundreds of Gops for low power embedded systems in a few years). New algorithms and new technologies introduce dynamic reconfiguration system on chip in the design flow. If the design productivity does not increase dramatically, the limiting factor of the growth of the semiconductor industry will not be the physical limitations due to the thinness of the fabrication process but the economy! Indeed we ask to the system design teams to build more complex systems faster, cheaper, bug free and decreasing the power consumption...

We propose in the DaRT project to contribute to the improvement of the productivity of the electronic embedded system design teams. We structure our approach around a few key ideas:

- Promote the use of *parallelism* to help reduce the power consumption while improving the performance.
- Use of *MDE(Model Driven Engineering)* By separating the concerns in different models allowing reuse of these models and to keep them human readable.
- Propose an environment starting at the highest level of abstraction, namely the *system modeling* level.
- *Automate code production* by the use of (semi)-automatic *model transformations* to build correct by construction code.
- Develop *simulation techniques* at precise abstraction levels (functional, transactional or register transfer levels) to check the design the soonest.
- Prototype the resulting embedded systems of FPGA and dynamically reconfigurable FPGA.
- Promote *strong semantics* in the application model to allow verification, non ambiguous design and automatic code generation.
- Focus on a *limited application domain*, intensive signal processing applications. This restriction allows us to push our developments further without having to deal with the wide variety of applications.

All these ideas are implemented into a prototype co-design environment based on a model driven engineering approach, Gaspard. This open source platform is our test bench and is freely available. To help the designer, such an environment should help to evaluate several architectural solutions as well as several application specifications with regard to their performance and cost. We are able to estimate metrics from SystemC simulations and the refactoring algorithm defined for the transformation of loops to particular multiprocessors are the first steps for exploration. Automatic exploration system based on multi-objective methods has to transform the SoC description (size, network, memory, association). The space of solutions is huge and a fast simulation in SystemC at a high abstraction level is a good opportunity to reduce the space in a short delay. After that, a precise simulation at low level in SystemC or even in VHDL (synthetizable VHDL) can start to refine the solution. Code production is also focussed for GPGPU using OpenCL language as an intermediary target.

The main technologies we promote are UML 2 [48] and MARTE profil, MDE [84] and Eclipse EMF [45] for the modeling and model handling; Array-OL [64], [65], [60], [58] and synchronous languages [56] as computation models with strong semantics for verification; SystemC [49] for the simulation; OpenMP for the shared memory parallel execution; OpenCL for the massively parallel GPU;VHDL for the synthesis; and Java to code our prototypes.

2.2. Highlights

([19]) received the Best Paper Award of the International Symposium on System-on-Chip (SoC 2010) in Tampere, Finland. http://soc.cs.tut.fi/2010/

3. Scientific Foundations

3.1. Introduction

The main research topic of the DaRT team-project concerns the hardware/software codesign of embedded systems with high performance processing units like DSP or SIMD processors. A special focus is put on multi processor architectures on a single chip (System-on-Chip). The contribution of DaRT is organized around the following items:

Co-modeling for High Performance SoC design: We define our own metamodels to specify application, architecture, and (software hardware) association. These metamodels present new characteristics as high level data parallel constructions, iterative dependency expression, data flow and control flow mixing, hierarchical and repetitive application and architecture models. All these metamodels are implemented with respect to the MARTE standard profile of the OMG group, which is dedicated to the modeling of embedded and real-time systems.

Model-based optimization and compilation techniques: We develop automatic transformations of data parallel constructions. They are used to map and to schedule an application on a particular architecture. This architecture is by nature heterogeneous and appropriate techniques used in the high performance community can be adapted. We developed new heuristics to minimize the power consumption. This new objective implies to specify multi criteria optimization techniques to achieve the mapping and the scheduling.

SoC simulation, verification and synthesis: We develop a SystemC based simulation environment at different abstraction levels for accurate performance estimation and for fast simulation. To address an architecture and the applications mapped on it, we simulate in SystemC at different abstraction levels the result of the SoC design. This simulation allows us to verify the adequacy of the mapping and the schedule, e.g., communication delay, load balancing, memory allocation. We also support IP (Intellectual Property) integration with different levels of specification. On the other hand, we use formal verification techniques in order to ensure the correctness of designed systems by particularly considering the synchronous approach. Finally, we transform MARTE models of data intensive algorithms in VHDL, in order to synthesize a hardware implementation.

3.2. Co-modeling for HP-SoC design

The main research objective is to build a set of metamodels (application, hardware architecture, association, deployment and platform specific metamodels) to support a design flow for SoC design. We use a MDE (Model Driven Engineering) based approach.

3.2.1. Foundations

3.2.1.1. System-on-Chip Design

SoC (System-on-Chip) can be considered as a particular case of embedded systems. SoC design covers a lot of different viewpoints including the application modeling by the aggregation of functional components, the assembly of existing physical components, the verification and the simulation of the modeled system, and the synthesis of a complete end-product integrated into a single chip.

The model driven engineering is appropriate to deal with the multiple abstraction levels. Indeed, a model allows several viewpoints on information defined only once and the links or transformation rules between the abstraction levels permit the re-use of the concepts for a different purpose.

3.2.1.2. Model-driven engineering

Model Driven Engineering (MDE) [84] is now recognized as a good approach for dealing with System on Chip design issues such as the quick evolution of the architectures or always growing complexity. MDE relies on the model paradigm where a model represents an abstract view of the reality. The abstraction mechanism avoids dealing with details and eases reusability.

A common MDE development process is to start from a high level of abstraction and to go to a targeted model by flowing through intermediate levels of abstraction. Usually, high level models contain only domain specific concepts, while technological concepts are introduced smoothly in the intermediate levels. The targeted levels are used for different purposes: code generation, simulation, verification, or as inputs to produce other models, etc. The clear separation between the high level models and the technological models makes it easy to switch to a new technology while re-using the previous high level designs. Transformations allow to go from one model at a given abstraction level to another model at another level, and to keep the different models synchronized

In an MDE approach, a SoC designer can use the same language to design application and architecture. Indeed, MDE is based on proved standards: UML 2 [47] for modeling, the MOF (Meta Object Facilities [80]) for metamodel expression and QVT [81] for transformation specifications. Some profiles, i.e. UML extensions, have been defined in order to express the specificities of a particular domain. In the context of embedded system, the MARTE profile in which we contribute follows the OMG standardization process.

3.2.1.3. Models of computation

We briefly present our reference models of computation that consist of the Array-OL language and the synchronous model. The former allows us to express the parallelism in applications while the latter favors the formal validation of the design.

Array-OL. The Array-OL language [64], [65], [60], [58] is a mixed graphical-textual specification language dedicated to express multidimensional intensive signal processing applications. It focuses on expressing all the potential parallelism in the applications by providing concepts to express data-parallel access in multidimensional arrays by regular tilings. It is a single assignment first-order functional language whose data structures are multidimensional arrays with potentially cyclic access.

The synchronous model. The synchronous approach [56] proposes formal concepts that favor the trusted design of embedded real-time systems. Its basic assumption is that computation and communication are instantaneous (referred to as "synchrony hypothesis"). The execution of a system is seen through the chronology and simultaneity of observed events. This is a main difference from visions where the system execution is rather considered under its chronometric aspect (i.e., duration has a significant role). There are different synchronous languages with strong mathematical foundations. These languages are associated with tool-sets that have been successfully used in several critical domains, e.g. avionics, nuclear power plants.

In the context of the DaRT project, we consider declarative languages such as Lustre [62] and Signal [76] to model various refinements of Array-OL descriptions in order to deal with the control aspect as well as the temporal aspect present in target applications. The first aspect is typically addressed by using concepts such as mode automata, which are proposed as an extension mechanism in synchronous declarative languages. The second aspect is studied by considering temporal projections of array dimensions in synchronous languages based on clock notion. The resulting synchronous models are analyzable using the formal techniques and tools provided by the synchronous technology.

3.2.2. Contributions of the team

Our proposal is partially based upon the concepts of the "Y-chart" [69]. The MDE contributes to express the model transformations which correspond to successive refinements between the abstraction levels.

Metamodeling brings a set of tools which enable us to specify our application and hardware architecture models using UML tools, to reuse functional and physical IPs, to ensure refinements between abstraction levels via mapping rules, to initiate interoperability between the different abstraction levels used in a same codesign, and to ensure the opening to other tools, like verification tools, thought the use of standards.

The application and the hardware architecture are modeled separately using similar concepts inspired by Array-OL to express the parallelism. The placement and scheduling of the application on the hardware architecture is then expressed in an association model.

All the previously defined models, application, architecture and association, are platform independent and they conform to the MARTE OMG Profil (figure 1). No component is associated with an execution, simulation or synthesis technology. Such an association targets a given technology (OpenMP, OpenCL, SystemC/PA, VHDL, etc.). Once all the components are associated with some IPs of the GasparLib library, the deployment is fully realized. This result can be transformed to further abstraction level models via some model transformations (figure 2).

The simulation results can lead to a refinement of the initial application, hardware architecture, association and deployment models. We propose a methodology to work with all these different models. The design steps are:

1. Separation of application and hardware architecture modeling.
2. Association with semi-automatic mapping and scheduling.
3. Selection of IPs from libraries for each element of application/architecture models, to achieve the deployment.
4. Automatic generation of the various platform specific simulation or execution models.
5. Automatic simulation or execution code generation with calls to the IPs.
6. Refinement at the highest level taking account of the simulation results.

3.2.2.1. High-level modeling in Gaspard2

In Gaspard2, models are described by using the recent OMG standard MARTE profile combined with a few native UML concepts and some extensions.

The new release of Gaspard2 uses different packages of MARTE for UML modeling. The Hardware Resource Model (HRM) concepts of MARTE enable to describe the hardware part of a system. The Repetitive Structure Modeling (RSM) concepts allow one to describe repetitive structures (DaRT team was the main contributor of this MARTE package definition). Finally, the Generic Component Modeling (GCM) concepts are used as the base for component modeling.

The above concepts are expressive enough to permit the modeling of different aspects of an embedded system:

- functionality (or applicative part): the focus is mainly put on the expression of data dependencies between components in order to describe an algorithm. Here, the manipulated data are mainly multidimensional arrays. Furthermore, a form of reactive control can be described in modeled applications via the notion of execution modes. This last aspect is modeled with the help of some native UML notions in addition to MARTE.
- hardware architecture: similar mechanisms are also used here to describe regular architectures in a compact way. Regular parallel computation units are more and more present in embedded systems, especially in SoCs. HRM is fully used to model these concepts. Some extensions are proposed for NoC design and FPGA specifications. The GPU have a particular memory hierarchy. In order to model the memory details, we extend the MARTE metamodel to describe low level characteristics of the memory.
- association of functionality with hardware architecture: the main issues concern the allocation of the applicative part of a system onto the available computation resources, and the scheduling. Here also, the allocation model takes advantage of the repetitive and hierarchical representation offered by MARTE to enable the association at different granularity levels, in a factorized way.

In addition to the above usual design aspects, Gaspard2 also defines a notion of *deployment* specification (see Figure 1) in order to select compilable IPs from libraries, at this time models can produce codes. The corresponding package defines concepts that (i) enable to describe the relation between a MARTE representation of an elementary component (a box with ports) to a text-based code (and Intellectual Property - IP, or a function with arguments), and (ii) allow one to inform the Gaspard2 transformations of specific behaviors of each component (such as average execution time, power consumption...) in order to generate a high abstraction level simulation in adequacy with the real system. Recently this package was extended to design reconfigurable systems using dynamical deployment.

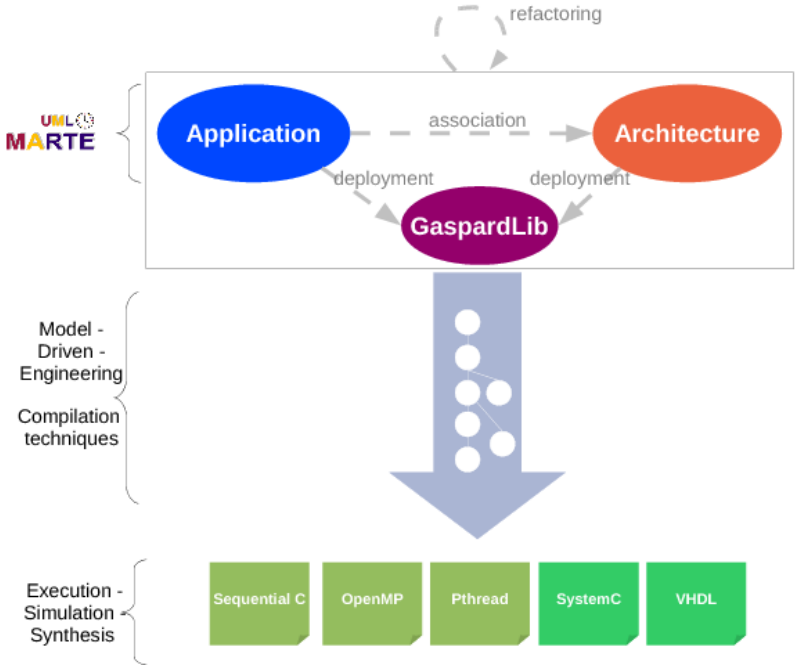

Figure 1. Overview of the design concepts.

3.2.2.2. Intermediate concept modeling and transformations

Gaspard2 targets different technologies for various purposes: formal verification, high-performance computing, simulation and hardware synthesis (Figure 1). This is achieved via model transformations that relate intermediate representations towards the final target representations.

- A metamodel for procedural language with OpenMP (OpenMP in Figure 1). It is inspired by the ANSI C and Fortran grammars and extended by OpenMP statements [50]. The aim of this metamodel is to use the same model to represent Fortran and C code. Thus, from an OpenMP model, it is possible to generate OpenMP/Fortran or OpenMP/C. The generated code includes parallelism directives and control loops to distribute task (IPs code) repetitions over processors [87].
- A VHDL metamodel (VHDL in Figure 1). It gathers the necessary concepts to describe hardware accelerators at the RTL (Register Transfer Level) level, which allows the hardware execution of applications. This metamodel introduces, *e.g.*, the notions of *clock* and *register* in order to manipulate some of the usual hardware design concepts. It is precise enough to enable the generation of synthetizable HDL code [75].

- The two metamodels SystemC and Pthread was redefined to implement both a multi-thread execution model. These are described in the " New results" part.
- Synchronous metamodel (Synchronous Equational). It was used to benefit of the verification tools of synchronous languages. It is not yet maintained in the new release of Gaspard2.

The transformation scheme. In order to target these metamodels, several transformations have been developed (Figure 2). *MartePortInstance* introduces into the MARTE metamodel the concept of *PortInstance* corresponding to an instance of port associated to a part. The *ExplicitAllocation* transformation explicits the association of each application part on the processing units, according to the association of other elements in the application hierarchy. The *LinkTopologyTask* transformation replaces the connectors between a component and an inner repeated part by a task managing the data (*TilerTask*). The scheduling of the application tasks is decomposed into three transformations, *Synchronisation* that associates, to each application component, a local graph of tasks corresponding to its parts; *GlobalSynchronization* that computes a global graph of tasks for the complete application from the local graphs of tasks; and *Scheduling* that schedules the tasks from the global graph. *TilerMapping* maps the *TilerTasks* onto processors. The management of the data in the memory is performed through two transformations. *MemoryMapping* maps the data into memory *i.e.* creates the variables and allocates address spaces. *AddressComputation* computes addresses for each variable. Finally, some transformations are dedicated to targets: *Functional* introduces the concepts relative to procedural languages. *pThread* transforms MARTE elementary tasks into threads and the connectors into buffers. *SystemC* traduces the MARTE architecture into concepts of the SystemC language.

3.2.2.3. An operational semantics for RSM

The Repetitive Structure Modeling (RSM) package of the UML MARTE profile is used to describe repetitive computations and topologies (e.g., data-parallel algorithms, grid of processing units) in an embedded system. In Gaspard2, the concepts provided by this package are of prime importance for the specification of data-intensive applications. A formal semantics [59] has been previously defined for the Array-OL language, which is the basis for the definition of RSM. We proposed an new formal semantics for RSM, which is operational unlike [59]. Execution semantic descriptions are rarely taken into account in the definition of UML profiles. This raises several serious correctness issues about the manipulation of models defined with these profiles. The aim of our new semantics [31] is to answer this demand by proposing a help for understanding the behavior and execution of models specified with RSM concepts in UML MARTE.

3.2.2.4. Clock-based modeling of embedded system behavior

The concepts defined in the RSM package of MARTE allow one to suitably describe the data intensive algorithms [52] [51]. In order to add more details about the system functional behavior, logical clocks are associated with components to describe the expected rates at which data should be processed. The Time sub-profile of MARTE is used to model this rate information. It offers a rich expressivity for describing both logical and physical time aspects [54]. The rate constraints are expressed using the CCSL package of MARTE in the form of clock constraints. We refer to this clock constraints as functional clock properties.

The physical resources that implement the data intensive algorithms are specified in MARTE. For each resource, hardware IPs are deployed in order to refine the models towards a specific technology. At this level, we extract information concerning the processors speed represented by its frequency. We synthesize new clocks that represent the periods of the clock cycles for each processor involved in the execution. All clocks are related to an ideal clock. The occurrence of the instants of the ideal clock are fast enough to capture any instant of the processors clocks. We refer to these clock specifications as physical clock properties.

Since application functionality and hardware architecture are modeled independently in Gaspard2, the allocation phase bridges these two different views in order to map functionality on their associated physical resources. In terms of clocks, this allocation is expressed as the mapping of functional clock properties onto physical clock properties, according to a particular mapping algorithm. The result of such allocation is a new set of clocks reflecting the simulation of the temporal behavior of the system during execution. We refer to these clock description as simulation clock properties. They are usable for a very relevant system analysis.

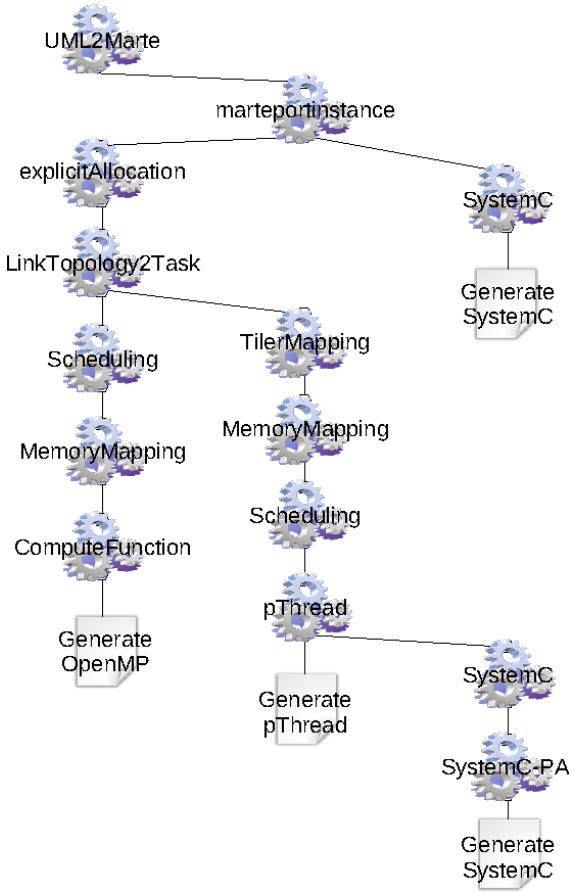

Figure 2. Overview of the transformation chains.

3.2.2.5. High-level modeling and exploration of non functional properties

We have proposed an approach for high-level modeling and exploration of non functional properties. Our work proposed a Model Driven Engineering (MDE)-based approach to integrate non functional requirements for systems on chip and defined metamodels that allow the integration of external optimization tools in the Gaspard2 environment. The designer creates the application and architecture models at a high level. The designer should then take the decision to allocate application functions on hardware components. This decision depends essentially on the non functional properties of both of the software and hardware components. For this reason, it is necessary to express these requirements. The proposed methodology uses models enriched with non-functional properties to drive the optimization of resource allocation.

3.2.2.6. HPF towards Marte

Concerning the power of expression of the MARTE RSM subprofile that we have defined, we have studied the data and computation distribution capabilities. We have proved that the MARTE «distribute» stereotype is at least as expressive as the well known High Performance Fortran data distribution. The proof is constructive: starting from an ALIGN and a DISTRIBUTE HFP directive, we build a MARTE «distribute».

3.3. Model-based optimization and compilation techniques

3.3.1. Foundations

3.3.1.1. Optimization for parallelism

We study optimization techniques to produce "good" schedules and mappings of a given application onto a hardware SoC architecture. These heuristic techniques aim at fulfilling the requirements of the application, whether they be real time, memory usage or power consumption constraints. These techniques are thus multi-objective and target heterogeneous architectures.

We aim at taking advantage of the parallelism (both data-parallelism and task parallelism) expressed in the application models in order to build efficient heuristics.

Our application model has some good properties that can be exploited by the compiler: it expresses all the potential parallelism of the application, it is an expression of data dependencies –so no dependence analysis is needed–, it is in a single assignment form and unifies the temporal and spatial dimensions of the arrays. This gives to the optimizing compiler all the information it needs and in a readily usable form.

3.3.1.2. Transformation and traceability

Model to model transformations are at the heart of the MDE approach. Anyone wishing to use MDE in its projects is sooner or later facing the question: how to perform the model transformations? The standardization process of Query View Transformation [81] was the opportunity for the development of transformation engine as Viatra, Moflon or Sitra. However, since the standard has been published, only few of investigating tools, such as ATL[1] (a transformation dedicated tool) or Kermeta [2] (a generalist tool with facilities to manipulate models) are powerful enough to execute large and complex transformations such as in the Gaspard2 framework. None of these engine is fully compliant with the QVT standard. To solve this issue, new engine relying on a subset of the standard recently emerged such as QVTO [3] and smartQVT. These engines implement the QVT Operational language.

Traceability may be used for different purposes such as understanding, capturing, tracking and verification on software artifacts during the development life cycle [70]. MDE has as main principle that everything is a model, so trace information is mainly stored as models. Solutions are proposed to keep the trace information in the initials models source or target [88]. The major drawbacks of this solution are that it pollutes the models with additional information and it requires adaptation of the metamodels in order to take into account traceability. Using a separate trace model with a specific semantics has the advantage of keeping trace information independent of initial models [72].

[1] http://www.eclipse.org/m2m/atl
[2] http://www.kermeta.org
[3] http://www.eclipse.org/m2m/qvto/doc

3.3.2. Contributions of the team

3.3.2.1. Data-parallel code transformations

We have studied Array-OL to Array-OL code transformations [60], [85], [67], [66], [68] [71]. Array-OL allows a powerful expression of the data access patterns in such applications and a complete parallelism expression. It is at the heart of our metamodel of application, hardware architecture and association.

The code transformations that have been proposed are related to loop fusion, loop distribution or tiling but they take into account the particularities of the application domain such as the presence of modulo operators to deal with cyclic frequency domains or cyclic space dimensions (as hydrophones around a submarine for example).

We pursue the study of such transformations with two objectives:

- Propose utilization strategies of such transformations in order to optimize some criteria such as memory usage, minimization of redundant computations or adaptation to a target hardware architecture.
- Stretch their application domain to our more general application model (instead of just Array-OL).

In 2009 the study on the interaction between the high-level data-parallel transformations and the inter-repetition dependencies (allowing the specification of uniform dependencies) was achieved. Because the ODT formalism behind the Array-OL transformations cannot express dependencies between the elements of the same multidimensional space, in order to take into account the uniform dependencies we proposed and proved an algorithm that, starting from the hierarchical distribution of repetition before and after a transformation, is capable to compute the new uniform dependencies that express the same exact dependencies as before the transformations. It all comes down to solving an (in)equations system, interpreting the solutions and translating them into new uniform dependencies.

The algorithm was implemented and integrated into the refactoring toolbox and enables the use of the transformations on models containing inter-repetition dependencies.

In order to validate the theoretical work around the high-level Array-OL refactoring based on the data-parallel transformations, together with Eric Lenormand and Michel Barreteau from THALES Research & Technology we worked on a study on optimization techniques in the context of an industrial radar application. We have proposed a strategy to use the refactoring toolbox to help explore the design space, illustrated on the radar application modeled using the Modeling and Analysis of Real-time and Embedded systems (MARTE) UML profile.

3.3.2.2. Multi-objective hierarchical scheduling heuristics

When dealing with complex heterogeneous hardware architectures, the scheduling heuristics usually take a task dependence graph as input. Both our application and hardware architecture models are hierarchical and allow repetitive expressions. We propose a Globally Irregular, Locally Regular (GILR) combination of heuristics to allow to take advantage of both task and data parallelism [77] and have started evaluating multi-objective evolutionary meta-heuristics in this context. These evolutionary meta-heuristics deal with the irregular (task parallelism) part of the design [57] while we have proposed a heuristic to deal with the regular part (data parallelism) [78].

Furthermore, local optimizations (contained inside a hierarchical level) decrease the communication overhead and allow for a more efficient usage of the memory hierarchy. We aim at combining the data-parallel code transformations presented before and the GILR heuristics in order to deal efficiently with the data-parallelism of the application by using repetitive parts of the hardware architecture.

The introduction of uniform inter-repetition dependencies in the data-parallel tasks of Gaspard2 has had several consequences. Aside the modification of the refactoring (see section 3.3.2.1), we have studied the compilation of such tasks. This compilation involves the scheduling of such repetitions on repetitive grids of processors and the code generation. This scheduling problem is NP-complete and we have proposed a

heuristic based on the automatic parallelization techniques to compute a good (efficient both in time and code size) schedule in the case when all loop bounds and processor array shapes are known.

3.3.2.3. Transformation techniques

In the previous version of Gaspard2, model transformations were complex and monolithic. They were thus hardly evolvable, reusable and maintainable. We thus proposed to decompose complex transformations into smaller ones jointly working in order to build a single output model [29]. These transformations involve different parts of the same input metamodel (e.g. the MARTE metamodel); their application field is localized. The localization of the transformation was ensured by the definition of the intermediary metamodels as delta. The delta metamodel only contains the few concepts involved in the transformation (i.e. modified, or read). The specification of the transformations only uses the concepts of these deltas. We defined the Extend operator to build the complete metamodel from the delta and transposed the corresponding transformations. The complete metamodel corresponds to the merge between the delta and the MARTE metamodel or an intermediary metamodel. The transformation then becomes the chaining of metamodel shifts and the localized transformation. This way to define the model transformations has been used in the Gaspard2 environment. It allowed a better modularity and thus also reusability between the various chains.

3.3.2.4. Traceability

Our traceability solution relies on two models the Local and the Global Trace metamodels. The former is used to capture the traces between the inputs and the outputs of one transformation. The Global Trace metamodel is used to link Local Traces according to the transformation chain. The local trace also proposes an alternative "view" to the common traceability mechanism that does not refers to the execution trace of the transformation engine. It can be used whatever the used transformation language and can easily complete an existing traceability mechanism by providing a more finer grain traceability [20].

Furthermore, based on our trace metamodels, we developed algorithms to ease the model transformation debug. Based on the trace, the localization of an error is eased by reducing the search field to the sequence of the transformation rule calls [55].

3.3.2.5. Verifying conformance and semantics-preserving model transformations

We give formal executable semantics to the notions of *conformance* and of *semantics-preserving model transformations* in the model-driven engineering framework [83]. Our approach consists in translating models and meta-models (possibly enriched with OCL invariants) into specifications in *Membership Equational Logic*, an expressive logic implemented in the Maude tool. Conformance between a model and a meta-model is represented by the validity of a certain *theory interpretation*, of the specification representing the meta-model, in the specification representing the model. Model transformations between origin and destination meta-models are mappings between the sets of models that conform to the those meta-models, respectively, and can be represented by rewrite rules in *Rewriting Logic*, a superset of Membership Equational Logic also implemented in Maude. When the meta-models involved in a transformation are endowed with dynamic semantics, the transformations between them are also typically required to preserve those semantical aspects. We propose to represent the notion of dynamic semantics preservation by means of *algebraic simulations* expressed in Membership Equational Logic. Maude can then be used for automatically verifying conformance, and for automatically verifying dynamic semantics preservation up to a bounded steps of the dynamic semantics. These works lead to better understood meta-models and models, and to model transformations containing fewer errors.

3.3.2.6. Modeling for GPU

The model described in UML with Marte profile model is chained in several inout transformations that adds and/or transforms elements in the model. For adding memory allocation concepts to the model, a QVT transformation based on «Memory Allocation Metamodel» provides information to facilitate and optimize the code generation. Then a model to text transformation allows to generate the C code for GPU architecture. Before the standard releases, Acceleo is appropriate to get many aspects from the application and architecture model and transform it in CUDA (.cu, .cpp, .c, .h, Makefile) and OpenCL (.cl, .cpp, .c, .h, Makefile) files. For the code generation, it's required to take into account intrinsic characteristics of the GPUs like data distribution, contiguous memory allocation, kernels and host programs, blocks of threads, barriers and atomic functions.

3.4. HP-SoC simulation, verification and synthesis

Many simulations at different levels of abstraction are the key of an efficient design of embedded systems. The different levels include a functional (and possibly distributed) validation of the application, a functional validation of the application and an architecture co-model, and a validation of a heterogeneous specification of an embedded system (a specification integrating modules provided at different abstraction levels).

SoCs are more and more complex and integrate software parts as well as specific hardware parts (IPs, Intellectual Properties). Generally before obtaining a SoC on silicium, a system is specified at several abstraction levels. Any system design flow consists in refining, more or less automatically, each model to obtain another, starting from a functional model to reach a Register Transfer Level model. One of the biggest design challenges is the development of a strong, low cost and fast simulation tool for system verification and simulation.

The DaRT project is concerned by the simulation at different levels of abstraction (SystemC, VHDL) of the application/architecture co-model and of the mapping/schedule produced by the optimization phase.

3.4.1. Foundations

3.4.1.1. Abstraction levels and Transaction Level Modeling

Currently, Transaction Level Modeling, TLM, is being used in the industry to solve a variety of practical problems during the design, development and deployment of electronic systems.

The TLM 2.0 standard appeared during the very few last years. It consists in describing systems according to the specifications of the TLM abstraction levels. At these levels, function calls simulate the behavior of the communications between architecture components.

Nowadays, this modeling style is widely used for verification and it is starting to be used for design at many major electronic companies. Recently, many actions and challenges have been started in order to help to proliferate TLM. Thus, several teams are working to furnish to designers standard TLM APIs and guidelines, TLM platform IP and tools supports. SystemC is the first system description language adopting TLM specifications. Thus, several standardization APIs have been proposed to the OSCI by all the major EDA and IP vendors. This standardization effort is being generalized now by the OSCI / OCP-IP TLM standardization alliance, to build on a common TLM API foundation. One of the most important TLM API proposals is the one from Cadence, distributed to OSCI and OCP-IP. It is intended as common foundation for OSCI and OCP-IP allowing protocol-specific APIs (e.g. AMBA, OCP) and describing a wide range of abstraction levels for fast and efficient simulations.

In order to keep our design flow coherent, we choose to use two significant simulation levels. Each of them has special advantages.

The main objectives of the PVT level are fast verification of system functionalities and monitoring of the contentions in the interconnection network. Complementary to this level, the CABA level is used to accurately estimate the execution time and power consumption. At the PVT level, details related to the computation and communication resources are omitted. The software application is executed by an instruction-accurate Instruction Set Simulator. Transactions are performed through channels instead of signals. At the CABA level, hardware components are implemented at the cycle accurate level for both processing and communication parts. Communication protocol and arbitration strategy are specified as well. Simulation at the PVT level permits a rapid exploration of a large solution space by eliminating non interesting regions from the DSE process. The solutions selected at this level are then forwarded to a new exploration at the CABA level. At each level, the exploration is based on developed performance and power estimation tools. Code generation at both of those levels needs parameter specifications for execution time, power estimation, and platform configurations. These parameters are specified at the deployment phase.

Due to all TLM's benefits, we defined a TLM metamodel as a top level point for automatic transformations to both simulation and synthesis platforms. Our TLM metamodel contains the main concepts needed for verification and design following the Cadence API proposal. But, as we are targeting multi-language simulation

platforms, the meta model is completely independent from the SystemC syntax. It is composed mainly by two parts: architecture and application. This clear separation between SW and HW parts permits easy extensions and updates of the meta model.

- The architecture part contains all necessary concepts to describe HW elements of systems at TLM levels. The SW part is mainly composed of computation tasks. They should be hierarchical and repetitive. A set of parameters could be attached to each task in order to specify the scheduling dependently of the used computation model.
- Thus this metamodel keeps hierarchies and repetitions of both the application and the architecture. This permits to still benefit from the data parallelism as far as possible in the design (simulation and synthesis flow). In fact, the designer can choose to eliminate hierarchies when transforming the TLM model into a simulation model, and to keep it when transforming into a synthesis model.

3.4.1.2. Dynamic reconfiguration - FPGA

Current FPGAs support the notion of Partial Dynamic Reconfiguration which allows part of the FPGA to be reconfigured on the fly hence introducing the idea of virtual hardware. Partial Reconfiguration allows swapping of tasks (mutually exclusive)depending upon user requirements and Quality of service needs. Using such a technology permits to optimize energy consumption and the area in the system. It allows also to have very flexible systems, adaptable for large application classes.

3.4.1.3. Verification

Our privileged basis for verification is the reactive synchronous domain. Over the last two decades several formal verification technologies have been provided by a very active research community in this domain. Among the available tools, we can mention efficient compilers that act more than usual compilers in that they address more static analysis issues. There are also various model-checkers that use both symbolic representations and non symbolic ones. Some of these model-checkers offer facilities that go beyond verification by enabling the synthesis of (discrete) controllers. Finally, these synchronous technologies give the opportunity in some cases to perform a functional simulation of the described systems.

3.4.2. Contributions of the team

The results of DaRT simulation package concerns mainly the PVT and the CABA levels. We also propose techniques to interact with IPs specified at other level of abstraction (mainly RTL).

3.4.2.1. Co-simulation in SystemC

From the association model, the Gaspard2 environment is able to automatically produce SystemC simulation code. The MDE techniques offer the transformation of the association model to the SystemC model. During this transformation the data parallel components are unrolled and the data dependencies between elementary tasks become synchronization primitive calls relying on a buffered strategy.

The SoC architecture is produced from the architecture model coupled with a ready-to-use component library. A processing module in SystemC simulates the behavior of tasks mapped to a particular processor.

Other modules contain the data parallel structures and are able to answer to any read/write requests. The communications between tasks and between tasks and memories are simulated via communication modules in SystemC. These last modules produce interesting results concerning the simultaneous network conflicts and the capacity of this network for this application.

A transformation chain within Gaspard2 ensures the code generation from the input model. The produced simulation code is based on SystemC IPs assembling. These IPs are available in the Gaspard2 library in both TLM and CABA levels. They represent all the usual architecture components such as processors (ARM, MIPS, ..etc), memories, caches, buses, NoCs, etc.

3.4.2.2. Model transformation towards Pthreads

The strategy in previous version of the Gaspard2 framework imposed a global synchronization mechanism between all the tasks of the application. This mechanism does not allow one to reach an optimal execution. We have investigated a new strategy to overcome this problem, based on fine grain synchronizations between the different tasks of the modeled application. For this new strategy, we use the pthread API. Each task of the UML application model is transformed into a thread. The data exchanges between the tasks are ensured by a buffer-based strategy. The best compromise between the memory used and the performance can be reached by adjusting the size of each buffer. Moreover, we have developed this strategy to facilitate its use in simulation targets such as SystemC-PA. The transformation chain towards Pthreads enabled to optimize the global synchronization mechanism between all the tasks of the application provided by the previous version of Gaspard2.

3.4.2.3. Gaspardlib extensions

The chain towards SystemC code allows simulations at the TLM-PA level. Regarding the architecture design, the process acts at as a connector between existing SystemC modules. They correspond to basic components such as memories, processors, caches. They are gathered in the Gaspardlib to be included or linked at the code compilation step. On one hand, both application and architecture IPs have been modeled using UML to easily drag and drop the available components inside the user?s model. On another hand, we aimed at providing the most flexible design for the SystemC architecture.

The GaspardLib allows a high interoperability for our SystemC components with any other SystemC architecture. Consequently, additional SystemC modules have been integrated to extend the Gaspardlib. They come from other free simulation environments: ReSP,SocLib (https://www.soclib.fr/trac/dev/wiki), Unisim (https://www.soclib.fr/trac/dev/wiki).

3.4.2.4. Partial and Dynamic Reconfiguration (PDR) implementations

Current Gaspard2 Model transformation chain to Register Transfer Level (RTL) allows to generate two key aspects of a partial dynamically reconfigurable system: namely the dynamically reconfigurable region and the code for the reconfiguration manager that carries out the switch between the different configurations of this dynamic region. For this, the MARTE metamodel has been extended to integrate concepts of UML state machines and collaborations, which help in creation of mode automata semantics at the high abstraction levels. Integration of these concepts in the extended MARTE metamodel helps in the respective model-to-model transformations.

Moreover, the high level application model has several building blocks: the elementary components, each associated to several available intellectual properties (IPs). The current deployment level has been also extended to integrate the notion of ”configurations”, which are unique global implementations of the application functionality, with each configuration comprised of different combinations of IPs related to the elementary components. Using a combination of the deployment level and the introduced control semantics, it is possible for a designer to change the configuration related to an application, resulting in different results such as consumed FPGA resources, reconfiguration times, etc. We incorporate two model-to-model transformations in our flow, first the UML2MARTE transformation, with integrated state machine and configuration concepts. This transformation results in an intermediate MARTE model, which is converted into an RTL model by the MARTE2RTL transformation. The application model is converted into several implementations of a dynamically reconfigurable hardware accelerator, along with the source code for the configuration switch.

Finally, the design flow has been validated in the construction of a dynamically reconfigurable delay estimation correlation modulethat is part of a complex anti-collision radar detection system in collaboration with IEMN Valenciennes. The simulation results from the different configurations correspond to an initial MATLAB result, validating the different configurations. Additionally change of IPs related to a key elementary component in the module resulted in different reconfiguration times proving methodology.

3.4.2.5. IP based configurable massively parallel processing SoC

A methodology and a tool chain to design and build IP-based configurable massively parallel architectures is proposed. The defined architecture is named mppSoC, massively parallel processing System on Chip. It is a

SIMD architecture composed of a number of processor elements (the PEs) working in perfect synchronization. A small amount of local and private memory is attached to each PE. Every PE is potentially connected to its neighbors via a regular network. Furthermore, each PE is connected to an entry of mpNoC, a massively parallel Network on Chip that potentially connects each PE to one another, performing efficient irregular communications. All the system is controlled by an Array Controller Unit (ACU). Our objective is to propose then a methodology to produce FPGA implementations of the mppSoC architecture.

The whole mppSoC architecture with its various components is implemented following an IP based design methodology. An implementation on FPGA, ALTERA StratixII 2s180, is proposed as a proof of feasibility. The architecture consists of general IPs (processor IPs, memory IPs, etc.) and specific IPs supplied with the mppSoC system (control IPs, etc.). Specific IPs are used as a glue to build the architecture. General IPs present a defined interface which must be respected by the designer if it wants to produce its own IP. For this kind of IPs we provide a library to alleviate their design. The designed architecture is configurable and parametric. In fact, to construct a mppSoC system, we assemble IPs to generate a FPGA configuration. The designer has to make different choices. He has to determine the different components in his architecture, for example if it contains an irregular communication network with a defined interconnection router or a neighborhood one or both. Since we propose a parametric architecture, he has to choose also some architectural parameters such as the number of PEs, the memory size and the topology of the neighborhood network if it exists. After fixing the architecture, the designer will choose then the basic IPs which will be used such as processor IP, interconnection network IP, etc. By this way, the user can choose the most appropriate mppSoC configuration satisfying his needs. To evaluate the proposed design methodology we have implemented different sized architectures with various configurations. We have also tested some examples of data parallel applications such as FIR, reduction, matrix multiplication, image rotation and 2D convolution. Through simulation results we can choose the most appropriate mppSoC configuration with the optimal performance metrics: execution time, FPGA resources and energy consumption. As a result we have proposed an IP based methodology for the construction of mppSoC system helping the designer to choose the best configuration for a given application. It is a first step towards a mppSoC architecture exploration.

Ongoing work aims at integrating the mppSoC in a real application such a video processing framework. Future work will aim at improving the proposed IP assembling methodology to construct mppSoC systems. Our ultimate goal is to provide a completely tool to generate a mppSoC configuration in order to help the designer in a semi-automatic architecture exploration for a given application.

3.4.2.6. Caches in MPSoCs

In Multi-Processor System-on-Chip (MPSoC) architectures using shared-memory, caches plays an important impact on performance and energy consumption levels.

When the executed application depicts a high degree of reference locality, caches may reduce the amount of shared-memory accesses and data transfers on the interconnection network. Hence, execution time and energy consumption can be greatly optimized. However, caches in MPSoC architectures put forward the data coherency problem. In this context, most of the existing solutions are based either on data invalidation or data update protocols. These protocols do not consider the change in the application behavior. This paper presents a new hybrid cache-coherency protocol that is able to dynamically adapt its functioning mode according to the application needs.

An original architecture which facilitates this protocol's implementation in Network-On-Chip based MPSoC architectures has been proposed. Performances, in terms of speed up factor and energy reduction gain of the proposed protocol, have been evaluated using a Cycle Accurate Bit Accurate (CABA) simulation platform. Experimental results in comparison with other existing solutions show that this protocol may give significant reductions in execution time and energy consumption can be achieved.

3.4.2.7. Verification

Guaranteeing the correctness of systems is a highly important issue in the Gaspard2 design methodology. This is required at least for their validation. In order to provide the designer with the required means to cope with

validation, we propose to bridge the gap between the Gaspard2 design approach and validation techniques for SoCs by using the synchronous approach and test-based techniques.

We have already defined a synchronous dataflow equational model of Gaspard2 specification concepts. The resulting model is then usable to address various correctness issues: causality analysis that enables to detect erroneous data dependencies (i.e., those which lead to cycles) in specifications, clock synchronizability analysis when such a system model is to be considered on a deployment platform, etc.

Starting from the simulation clock properties of an embedded system (as described previously), we start an analysis of the system behavior. On the one hand, we verify whether or not the functional clock constraints specified by the designer in the application specification are met during the system execution on considered physical resources. When these constraints are not met, the simulation clock traces can be used to reason and find the solutions to satisfy the constraints. For instance, this may amount to decrease the speed of processors that compute data very fast or to increase the speed of processors that compute data very slowly. The modification of the processors speed by increasing or decreasing the speed should always respect the functional constraints imposed by the designer. It appears in the simulation clock traces by determining new physical clock properties from the suitable processor frequencies. Another example of solution may consist in delaying the first activation of a faster processor until an adequate time to begin the execution. Such an activation delay could be seen as minimizing the voltage/frequency. The team examples have highlighted some needs for a better numeric verification of synchronous programs, and we also work on the amelioration of precision of the Signal analysis.

4. Application Domains

4.1. Intensive signal processing

The DaRT project-team aims at improving the design of embedded systems with a strong focus on intensive signal processing applications.

This application domain is the most intensive part of signal processing, usually composed of systematic signal processing followed by intensive data processing. The systematic signal processing mainly consists of a chain of filters and regular processing applied on the input signals independently of the signal values. It results in a characterization of the input signals with values of interest. The intensive data processing applies irregular computations on these values of interest. Those computations may depend on the signal values.

Below are three application examples from our industrial partners.

Software Radio Receiver. This application is structured in a front end systematic signal processing including signal digitalizing, channel selection, and application of filters to eliminate interferences. These first data are decoded in a second and more irregular phase (synchronization, signal demodulation...).

Sonar Beam Forming. A classical sonar chain consists in a first and systematic step followed by a more general data processing. The first step provides frequency and location correlations (so called *beam*) from a continuous flow of data delivered by the hydrophones (microphones disposed around a submarine). It is based on signal elementary transformations: FFT (Fast Fourier Transformation) and discrete integration. The second step analyzes a given set of beams and their history to identify temporal correlation and association to signal sources.

Video Encoder/Decoder. A video encoder works in a two-steps approach. The first part (from preprocessing to wavelet/cosine decomposition) is systematic. The second part of the encoder includes irregular processing (quantification, coding stages, motion detection). The decoder works the other way around: a first irregular phase is followed by a systematic phase. Recently we have used the H264 protocol.

4.2. Transport

The automotive industry has specific problems, particularly due to increased safety requirements and legal framework. Some of these electronic systems have the potential to endanger the safety of vehicle occupants or other road users should an error or a mis-operation occur.

We modeled a cruise control connected to the satellite positioning system, GPS. From a UML specification and using classical verification and model checking techniques, we assured the correct behavior of the system. The codes are generated using FPGA devices. Moreover, as Gaspard2 is based on metamodels and transformations between metamodels, new algorithms or new FPGAs can rapidly be integrated in the system by the re-use of existing functional blocks.

4.3. High-performance computing

Using the OpenMP/Fortran code generation chain, we have experimented the generated code in a typical operation in the scientific field: the matrix multiplication. We have compared generated code with optimized BLAS library function. Different algorithms have been generated: row-column multiplication, multiplication by block, multiplication by block using optimized BLAS function for the sequential part. Those algorithms have been compared with the sequential BLAS function and the parallel BLAS function. The results [87] show that the way to use Gaspard2 in the High Performance Computing field is to entrust Gaspard2 to manage parallelism and to use optimized function for the sequential part.

4.4. Avionic test applications

Nowadays, high performance applications such as the one used in networking, aerospace, and defense are becoming more and more complex. Rather then the aspects that involve the high complexity of the data structures and the potential parallelism, this field of applications is also characterized by an adaptive behavior depending on the environment. Hence, hardware designers are stressed to define attractive architectures that must structurally adapt to meet hard real-time requirements. Traditional target architectures may be constructed of high general-purpose CPU's with associated specific hardware processing elements. However, these architectures cannot be adequate to support the complexity of future high performance applications since they are too slow to execute the software. Recently, in an attempt to improve performances, target systems are built on a heterogeneous computing platform including configurable hardware on programmable logic devices such as FPGA's (Field Programmable Gate Arrays). FPGA's have the ability to implement arbitrary hardware functions. With the new technologies, these devices can also be reprogrammed dynamically to change the implemented functionality. This characteristic nature makes FPGA's a good choice for the design of high performance applications where flexibility is needed. For, instance multiple processing functions may be allocated dynamically to the general-purpose CPU's or FPGA's on-the-fly or during system operation as the application requirements change. In this way, dynamic reconfigurable computing systems are promising in the aspect of powerful, flexible, and adaptive execution platforms for high performance applications. The main challenge of hybrid (CPU/FPGA) architectures concerns the programming model and the design methodology. We need to deal with the heterogeneity of both hardware and software parts in order to obtain a fast system prototyping. In current industrial practice, manual coding is still widely adopted in the development of hybrid architectures, which is clearly not suited to manage the complexity intrinsic in these systems. For designers, this approach is very tedious, error-prone and expensive. To overcome this challenge, we propose the usage of the Model-Driven Engineering (MDE) approach developed in Gaspard2 in the specific context of CPU/FPGA hybrid system design. The objective is to upgrade Gaspard2 to turn automatically a high level specification of the system into an executable implementation.

4.5. Electrical engine simulations

Within a collaboration with the L2EP, Abdellatif Tinzefte started to model and program a parallel version of a Maxwell equations solver based on a Finite Element Method (FEM) formulation, and the first step of this work is defining a parallel preconditioner for the Krylov solver. The idea here is to use the Finite Integration

Technique (FIT) in order to compute the electromagnetic phenomena as like the FEM but on a coarser grid. The F.I.T is efficient if the mesh is generated by hexahedron elements. With this regular mesh the obtained system is large, sparse and have some properties of regularity which can be used for the parallel computing. Thus this FIT parallel solver will be used to approach the FEM operator. The first numerical results show an excellent precision and a good acceleration for the FEM solver. Another part of this work, is to was implemented in CUDA and OpenCL as well a solver for Maxwell's equations (Finite-Element Method and a conjugate gradient). The aim is to accelerate and verify the parallel code on GPUs. The first results showed a speedup around 6 times against sequential code on CPU. Another approach uses an algorithm that explores the sparse matrix storage format (by rows and by columns). This one did not increase the speedup but it allows to evaluate the impact of different accesses to the memory.

5. Software

5.1. Gaspard2

Participant: Pierre Boulet [contact person].

Gaspard2 is an Integrated Development Environment (IDE) for SoC visual co-modeling. It allows or will allow modeling, simulation, testing and code generation of SoC applications and hardware architectures.

Its purpose is to provide a single environment for all the SoC development processes:

- High level modeling of applications and hardware architectures
- Application and hardware architecture association (mapping and scheduling)
- Application refactoring
- Deployment specification
- Model to model transformation (to automatically produce models for several target platforms)
- Code generation
- Simulation
- Reification of any stages of the development

The Gaspard2 tool is based on the Eclipse [44] IDE. A set of plugins provides the different functionalities. Gaspard2 provides an internal engine to execute transformation chains. This engine is able to run either QVT (OMG standard) or Java transformations. It is also able to run model-to-text transformations based on Acceleo [46]. The Gaspard2 engine is defined to execute models conform to an internal transformation chains meta-model. A GUI has been developed to specify transformation chain models by drawing them.

For the final user, application, hardware architecture, association, deployment and technology models are specified and manipulated by the developer through UML diagrams, and saved by the UML tool in an XMI file format. Gaspard2 manipulates these models through repositories (Java interfaces and implementations) automatically generated thanks to the Ecore specification. Several transformation chains are provided with Gaspard2 to target, from UML models, several execution or simulation platforms (OpenMP, OpenCL, Pthread, SystemC, VHDL, ...). This input language is based on the MARTE UML profile.

A tool to generate SIMD configurations derived from the mppSoC model was developed. It allows to automatically generate the VHDL code from a high specification modeled at a high abstraction level (UML model using MARTE profile) based on the IP mppSoC library. The developed tool facilitates to the user to choose a SIMD configuration adapted to his application needs. It has been integrated in the Gaspard environment.

Gaspard2 as an educational resource. The Gaspard2 platform was one of the topics taught in the context of the courses on embedded systems in Telecom Lille and in a Master 2 (TNSI) lecture " Design tools for embedded systems" at the University of Valenciennes. These lectures focused on the potentiality to generate several targets from a subset of the Marte profile and the ability to target system on chip architectures at the TLM level respectively. Furthermore, the model driven engineering characteristics of Gaspard2 are largely detailed in the lecture of Software engineering at Polytech Lille and in the Master of research at university of Lille too.

5.2. Papyrus

Participant: Cédric Dumoulin [contact person].

The Papyrus tool is an UML Development Environment fully compliant with the UML standard and providing all UML diagrams. It is now an Eclipse project (in the incubator state). (http://www.eclipse.org/modeling/mdt/?project=papyrus#papyrus). A first version of Papyrus Eclipse has been released with the Eclipse Helios train (mid 2010). The fully functional Papyrus I version still available (http://www.papyrusuml.org)

The Papyrus Tool is developed under an Open source license in collaboration with CEA, Atos, Obeo, Airbus, Prodevelop, Integranova.

5.3. MDFactory

Participants: Alexis Muller [contact person], Anne Etien, Thomas Legrand.

MDFactory is a Model Driven Engineering environment to design, develop and run software production chains. This tool supports our approach based on localized transformation and our Extend operator [REF]. It provides a graphical editor to build such production chains with drag and drop from a reusable transformation library. MDFactory is based on the Eclipse platform and the Eclipse Modeling Framework (EMF). It is used to build Gaspard2 integrated transformation chains.

6. New Results

6.1. Co-modeling for HP-SoC design

6.1.1. MARTE extensions for reconfigurable based systems

Reconfigurable FPGA based Systems-on-Chip (SoC) architectures are increasingly becoming the preferred solution for implementing modern embedded systems. However due to the tremendous amount of hardware resources available in these systems, new design methodologies and tools are required to reduce their design complexity.

In previous work, we provided an initial contribution to the modeling of these systems by extending MARTE profile to incorporate significant design criteria such as power consumption.

In its current version, MARTE lacks dynamic reconfiguration concepts. Even these later are necessary to model and implement rapid prototypes for complex systems.

Our objective is to define all necessary concepts for dynamic reconfiguration issues regarding configuration latency, resources number, etc. Afterwards, these concepts will be integrated to MARTE to obtain an extended and complete profile, which can be called Reconfigurable MARTE (RecoMARTE).

Our current proposals permit us to model fine grain reconfigurable FPGA architectures with an initial extension of the MARTE profile to model Dynamic Reconfiguration at a high-level description.

Since a controller is essential for managing a dynamically reconfigurable region, we modeled a state machine at high abstraction levels using UML state machine diagrams. This state machine is responsible for switching between the available configurations.

As a future work, we will analyze the reconfigurable design flow of Xilinx from the design partitioning to the bitstream generation stage. It is a starting point for understanding how to generate configuration files. Then, we will extract relevant data to define our own design flow.

6.1.2. Traceability

We use the transformation mechanism to assist a tester in the mutation analysis process dedicated to model transformations. The mutation analysis aims to qualify a test model set. More precisely, errors are voluntary injected in transformation and the ability of the test models set to highlight these errors is analyzed. If the number of highlighted errors, *i.e.* if the test model set is not enough qualified, new models have to be added in order to raise the set quality [79]. Our approach relies on the hypothesis that it is easier to modify an existing model than to create a new one from scratch. The local trace, coupled to a mutation matrix, helps the tester to identify adequate test models and their relevant parts to modify in order to improve the test data set. We propose a semi-automation approach that can automatically generate new test model in some cases and efficiently assist the testers in others cases [21].

6.1.3. Transformation migration after metamodel evolution

Metamodels evolve because of several reasons such as design refinement and software requirement changes. When this happens, transformations defined in terms of those metamodels might become inconsistent and migration would be necessary. Due to the lack of methodology support, transformation migration is mostly ad hoc and manually performed. Besides, the growing complexity and size of transformations make this task difficult and error prone. We started works in this domain area. More specifically, on the one hand, we specify transformation consistency by defining the relationship between transformation and metamodels, we called it domain conformance. On the other hand, we propose a transformation migration process which describes the set of tasks that should be completed in order to re-establish consistency after metamodel evolution [32], [35].

6.1.4. Model transformation towards SystemC-PA

The buffered strategy developed for the transformation chain towards pThread has been kept to simulate the behavior of the application for the SystemC-PA simulation target. Mapped tasks are associated to threads themselves run on SystemC processing modules. Most of the thread contents (concepts, transformation and code generator) were reused and coupled with the SystemC contents dedicated to the architecture. A new model transformation has been developed to map the threads related to the application to the SystemC elements related to the architecture. The data accesses in the new SystemC-PA target are triggered off when the buffers (Pthread mechanisms) are requested. Those accesses are forwarded to the architecture through the TLM2 communication channels of the processors running the thread. The resulting transformation chain is available in the on-line Gaspard version (http://www.gaspard2.org).

6.2. Model-based optimization and compilation techniques

6.2.1. Clock-based design space exploration for SoCs

We have previously proposed an abstract clock-based modeling of data-intensive SoCs behaviors within the Gaspard2 framework [52] [51]. Both application functionality and hardware architecture are characterized in terms of clocks. Then, their allocation is also expressed as a projection of functional clock properties onto physical clock properties, according to a mapping choice. The result of such allocation is a new set of clocks reflecting the simulation of the temporal behavior of the system during execution.

This year, this approach has been applied to the design of the H.264 encoder on a multiprocessor hardware architecture using the standard MARTE profile [19]. The obtained model has been analyzed by considering abstract clocks. In particular, it has been shown that such clocks help to tackle design space exploration issues via a relevant modeling of different hardware/software mappings. The trade-off about processor frequency scaling, system functional properties and energy consumption has been addressed, via different hardware IP choices. This has been achieved via a qualitative reasoning on traces resulting from a scheduling of logical clocks, capturing functional properties, on physical clocks derived from processors frequency.

6.2.2. Optimized code generation from UML/MARTE models

Starting from the observation that some semantics (and thus some optimization possibilities) are lost when generating code in a programming language from a UML/MARTE model, the contribution of a thesis co-directed with the CEA LIST is an optimization at the model level followed by a translation to the GENERIC intermediate representation of the gcc compilation framework in order to allow more optimization, for the moment focusing on code size optimization.

6.2.3. Architecture exploration based on meta-heuristics

Some progress has been made on the proposal of meta-heuristics use for multi-objective mapping and scheduling. In collaboration with the Dolphin project-team of INRIA Lille - Nord Europe and LIFL we have modeled the association process of Gaspard2 as an optimization problem in order to solve it with a genetic algorithm based heuristic that has been implemented in the ParadisEO optimization framework. This new heuristics is currently being integrated in the Gaspard2 tool. Another work comparing heuristics based on the particle swarm and genetic algorithm meta heuristics has been proposed in collaboration with the computer science laboratory of Oran, Algeria, in continuation of our collaboration.

6.2.4. Architecture exploration for efficient data transfer and storage

A major point in embedded system design today is the optimization of communication structures, memory hierarchy and global synchronizations. Such an optimization is a time consuming and error-prone process, that requires a suitable automatic approach. We proposed an electronic system level framework to explore the data transfer storage micro-architecture and the synchronization of iterative data-parallel applications [38]. The aim is to define a methodology that can be a front-end for loop-based high level synthesis or interconnect hardware IPs in order to realize memory-centric MPSoCs. In Gaspard2, this will enable to assess various mappings of Array-OL models onto different kinds of target architectures.

Our solution starts from a canonical Array-OL representation and apply a set of transformations in order to infer an Application Specific architecture that masks the times to transfer data with the time to perform the computations. A customizable model of the target architecture including FIFO queues and double buffering mechanism is proposed. The mapping of a given image processing application onto this architecture is performed through a flow of Array-OL transformations aimed to improve the parallelism level and to reduce the size of the used internal memories. A method based on an integer partition is considered to reduce the space of explored transformations.

6.2.5. Multi-objective mapping and scheduling heuristics

Mohamed Akli Redjedal, univ. Lille 1 master, co-directed with Laetitia Jourdan form the Dolphin project-team of INRIA Lille - Nord Europe and LIFL. The work of Mohamed Redjedal has consisted in modeling the association process of Gaspard2 as an optimization problem in order to solve it with a genetic algorithm based heuristic. He has indeed modeled this multi-objective mapping and scheduling problem, proposed a heuristic and its implementation in the ParadisEO optimization framework. A 1st year master student from the univ. of Brussels has worked 6 weeks on the model driven export from Gaspard2 to the optimization heuristics proposed by Mohamed Redjedal

6.2.6. GPGPU code production

The solution of large, sparse systems of linear equations « Ax=b » presents a bottleneck in sequential code executing on CPU. To solve a system bound to Maxwell's equations on Finite Element Method (FEM), a version of conjugate gradient iterative method was implemented in CUDA and OpenCL as well. The aim is to accelerate and verify the parallel code on GPUs. The first results showed a speedup around 6 times against sequential code on CPU. Another approach uses an algorithm that explores the sparse matrix storage format (by rows and by columns). This one did not increase the speedup but it allows to evaluate the impact of the access to the memory.

6.2.7. From MARTE to OpenCL.

We have proposed an MDE approach to generate OpenCL code. From an abstract model defined using UML/MARTE, we generate a compilable OpenCL code and then, a functional executable application. As MDE approach, the research results provide, additionally, a tool for project reuse and fast development for not necessarily experts. This approach is an effective operational code generator for the newly released OpenCL standard. Further, although experimental examples use mono device(one GPU) example, this approach provides resources to model applications running on multi devices (homogeneously configured). Moreover, we provide two main contributions for modeling with UML profile to MARTE. On the one hand, an approach to model distributed memory simple aspects, i.e. communication and memory allocations. On the other hand, an approach for modeling the platform and execution models of OpenCL. During the development of the transformation chain, an hybrid metamodel was proposed for specifying of CPU and GPU programming models. This allows generating other target languages that conform the same memory, platform and execution models of OpenCL, such as CUDA language. Based on other created model to text templates, future works will exploit this multi language aspect. Additionally, intelligent transformations can determine optimization levels in data communication and data access. Several studies show that these optimizations increase remarkably the application performance.

6.2.8. Formal techniques for construction, compilation and analysis of domain-specific languages

The increasing complexity of software development requires rigorously defined *domain specific modelling languages* (DSML). Model-driven engineering (MDE) allows users to define their language's syntax in terms of *metamodels*. Several approaches for defining operational semantics of DSML have also been proposed [86], [63], [53], [61], [82]. We have also proposed one such approach, based on representing models and metamodels as algebraic specifications, and operational semantics as rewrite rules over those specifications [15], [17]. These approaches allow, in principle, for model execution and for formal analyses of the DSML. However, most of the time, the executions/analyses are performed via transformations to other languages: code generation, resp. translation to the input language of a model checker. The consequence is that the results (e.g., a program crash log, or a counterexample returned by a model checker) may not be straightforward to interpret by the users of a DSML. We have proposed in [42] a formal and operational framework for tracing such results back to the original DSML's syntax and operational semantics, and have illustrated it on SPEM, a language for timed process management.

6.3. HP-SoC simulation, verification and synthesis

6.3.1. System Level Power Modeling

Due to the ongoing nano-miniaturization in chip production, estimation of power consumption is becoming a critical metric in embedded system design. In current industrial and academic practices, power estimation using low-level CAD tools is still widely adopted. These low level tools are however inconvenient to manage the architecture of modern complex embedded systems. System level power estimation is considered a vital premise to cope with the critical design constraints. The keywords in our contribution are Hybridization and decorrelation between abstraction levels. The hybridization is applied here at 2 levels: granularity of activities used to develop the power models in one side and the level of the considered abstraction on the other side. If almost of studies focus on power estimation for a given abstraction level without overcoming the wall of speed/accuracy trade-off, the idea is to build up hybrid power estimation tool that gathers different abstraction levels of the system to grab the strict relevant data depending on the power estimation process step. Thus, designers build their systems by instantiating different hardware and software IPs (Intellectual Property) from existing libraries. The granularity of the used power models should be coherent with the design approach. In this work, we develop a hybrid system level power estimator for embedded systems. First, power models relying on Functional Level Power Analysis (FLPA) methodology is developed. Secondly, we forge the whole system into a fast simulation framework in order to obtain the system's power consumption data. The combination of the above parts yields to a relatively fast and accurate power estimation. Our experimental

results, performed on explicit embedded platform, show that obtained power estimation are less than 1% of error when compared to the measurements realized on the real system. In our work, we further extend the usage of higher abstraction level to speed up the estimation with the help of multigranularity of input data and phase sampling of the application. At the end, the proposed power estimation is 21 times faster than the detailed simulation with a marginal error of 1.5%.

6.3.2. Energy consumption driven dynamic reconfigurable execution model

As a continuation of our work on energy consumption estimation for Systems on Chip (SoC) at the Cycle Accurate Level using SystemC simulation, the aim of our current work is to ensure the adaptivity of SoCs regarding changes at run time of some operating conditions such as consumption constraints. This adaptivity is based on the reconfigurability on the Socs implemented on FPGAs. Here, the energy consumption estimation is not done during simulation anymore but during the execution of the application on the FPGA.

In order to be adaptive to runtime changes, the system architecture has to be changed accordingly. A possible change can be, for example, to change the parallelism degree or to change a processing algorithm in order to consume less energy. The decision of reconfiguring is taken after a negotiation between consumption monitors integrated in the system. This monitors are OCP- compliant, which allows them to be easily integrated and reused for different architectures thanks to the genericity and parametrability of this standard communication protocol.

Up to now, we have started implementing simple systems on FPGA supporting the dynamic reconfiguration taking the user inputs as a criterion of reconfiguration. We also implemented some interface adapters in order to facilitate the future integration of the OCP monitors in the system. As a future work, we intend to integrate the energy consumption as a criterion of reconfiguration using monitors. These monitors are supposed to take decisions of reconfiguration after negotiating between them. Therefore, we started by studying the negotiation used on software systems such as multi-agent systems. We will adapt this for our hardware architecture on FPGA.

6.3.3. Partial dynamic reconfiguration

Partial dynamic reconfiguration modeling [13], [34] permits to generate two key aspects of a partial dynamically reconfigurable system from high level modeled specifications: namely the dynamically reconfigurable region and the code for the reconfiguration manager that carries out the switch between the different configurations of this dynamic region. Once these aspects are generated using the model transformations, it is possible to use commercial simulation and synthesis tools to implement dynamic reconfiguration in state of the art FPGAs [13]. Currently the intermediate model transformation chain is being updated to make use of the newly introduced intermediate metamodels and model transformations developed by the DaRT team, in order to provide a uniform design flow. Similarly, optimizations related to RTL code generation using Acceleo are also continuing.

However, the MARTE compliant high level specifications lack the means to express architectural details at high abstraction levels. For this reason, an initial exploratory analysis was carried out in [27] that expands the MARTE hardware concepts to include aspects of reconfigurable architectures, and to introduce aspects such as power consumption at these high level models. These works can be described as an initial contribution to the ANR FAMOUS project.

Similarly, MARTE has recently introduced the notion of 'configurations', similar to those introduced in [13]. These concepts permit to express system configuration at the MARTE UML models, but lack guidelines and precise semantics. An overview of these concepts was presented in [33], which highlights some of the shortcomings of the present concepts and provides an alternative, as described in [13].

6.3.4. Network on Chip synthesis

The study of Networks on Chip (NoC) is a research field that primarily addresses the global communication in Systems-on-Chip (SoC). The selected topology and the routing algorithm play a prime role in the performance of NoC architectures. In order to handle the design complexity and meet the tight time-to-market constraints, it

is important to automate most of these NoC design phases. The use of MARTE in modeling such architectures may provide designers asset of high level concepts to obtain compact and reusable models in a fast way.

Thus we defined a new methodology for modeling concepts of NoC based Architectures. It aims to improve the effectiveness of the MARTE standard by clarifying some notations and extending some definitions in the standard, in order to allow modeling complex NoC architectures.

6.3.5. IP based configurable massively parallel processing SoC

Our mppSoC project proposed a methodology and tool chain to design and build IP-based configurable massively parallel architectures. A mppSoc architecture is a SIMD architecture composed of a number of processor elements working in perfect synchronization, the PEs. Each PE is potentially connected to its neighbors via a regular network. Furthermore, each PE is connected to an entry of mpNoC, a massively parallel Network on Chip that performs efficient irregular communications. All the system is controlled by an Array Controller Unit, the ACU.

The mppSoc project aims at the design and implementation of a given mppSoC architecture to fit the requirements of a given application. The mppSoC architecture model is then configurable and parametrizable and our chain produces FPGA implementations of the mppSoC architecture.

Our last contributions define a model-driven based generation chain integrated in the Gaspard environment. A mppSoC UML model is defined using using the MARTE profile. From this model, our chain allows the generation of the corresponding mppSoC synthetizable VHDL code that can be directly simulated or prototyped on FPGA. Targeting the DE2-70 FPGA board, we have been able to validate some mppSoC configurations running signal processing applications [ref]. This last works conclude Mouna Baklouti PhD thesis [ref].

6.4. Application domain dependant results

6.4.1. Gaspard2 for avionic hybrid test platform design

The emergence and the maturity of FPGA circuits for distributed and reconfigurable architectures offer the opportunity to explore real time problems in the field of avionic systems. FPGA becomes de facto a major processing element as same as general CPUs. As of now, the FPGA is widely used in the field of I/O component in order to connect the real equipment with the CPU host. Among the main features mapped into the FPGA in the original architecture, we quote the fast serial link and RAM IPs (Intellectual property) which are needed to ensure communication between CPU and FPGA. Additionally, the Base Time IP is needed for the global system synchronization. This minimal configuration based on FPGA can be duplicated several times and connected together to build bigger test system or a complete simulator. Eurocopter expectation for the above-described architecture is to prototype some models which can be eligible and relocated in the FPGA. The objective is to increase the performances of these models and to reduce the communication latencies by the means of embedding the different parts in the same chip. To do so, we studied in this first year a real avionic test loop in order to extract the complex models that will be implemented in the FPGA. Different hardware model configurations have been explored to reach an optimal well-balanced global system using the ML403 Virtex-4 Xilinx board. Different tradeoffs in terms of performance and resource occupation in the FPGA are obtained. Later, these results will be used for dynamically adapt the system functioning according to the available resources and performance requirements.

As a second part, we used the MARTE profile to represent an hybrid system (CPU/FPGA).In the MARTE specification, an application is a set of tasks connected through ports. Tasks are considered as mathematical functions reading data from their input ports and writing data on their output ports. This specification has been used to model the avionic test loop. In addition, MARTE allows describing the hardware architecture in a structural way. Typical components such as HwProcessor, HwFPGA and HwRAM can be specified with their non-functional properties. We used this subset of MARTE in order to represent an hybrid multiprocessor architecture. The main component of this architecture is composed of the Xeon-X3370 processor (multicore CPU) and the Virtex-4 Xilinx FPGA. Furthermore, MARTE provides the Allocate concept as well as the

concept specially crafted for repetitive structures Distribute. This latter concept gives a way to express regular distribution of tasks onto a set of processors or FPGA resources. The mapping step relies on two types of distribution (timeScheduling and spatialDistibution) depending on the target hardware platform (CPU/FPGA). The different models of our avionic test loop can be mapped onto the host multicore processor, the embedded processor (Microblaze) or the hardware resources in the FPGA.

6.4.2. Electromagnetic modeling

The Finite Integration Technique (F.I.T) is used to compute the phenomena. This technique is efficient if the mesh is generated by a regular hexahedron. Moreover the matrix system, obtained from a regular mesh can be exploited to use the parallel direct solver. In fact, in reordering the unknowns by the nested dissection method, it is possible to construct directly the lower triangular matrix with many processors without assembling the matrix system. During this year, we have implement a parallel direct solver which has good efficiency for a reasonable number of processors.

7. Contracts and Grants with Industry

7.1. Collaboration within the competitiveness pole I-Trans

I-Trans (http://www.i-trans.org/) is the official industrial cluster, which aims at bringing together major French actors in rail technology and innovative transport systems. Their needs in computation power are huge and thus the DaRT project strongly participates to this initiative through the collaborations with both concerned academic and industrial actors, to design a new GPU-based server which aims to reach the Petaflops performance.

In this direction, we already have many discussions with the leading partner of this project : GPUTech. These discussions lead to the build of a smaller pre-prototype for this machine, and also the design of a set of applications which should be modeled in Gaspard2 for this new platform. This is were the DaRT project strongly contribute with its experience in massively parallel architectures.

7.2. Collaboration with CEA List

A PhD thesis (Asma Charfi) is co-advised between our team and the CEA List on optimized code generation from MARTE models. The idea is that some information is lost when the code is generated from a high level model to code. The compiler then tries to find back this lost information to optimize the code. If these optimizations were taken care of at model level, the compiler would have a simplified task to do and we could expect improved performance.

A new PhD thesis (Amine El Kouhen) is co-advised between our team and the CEA List on the adaptation of UML Tools to the domain and to the design process. The idea is to provide customers with a UML tool adapted to its work, here, the design of embedded system. The tool customization is done with the help of models or profiles

DaRT and the CEA List also collaborate on the Papyrus UML project.

7.3. Collaboration EADS IW, and Eurocopter

The subject deals with dynamic reconfigurable system design for avionic test applications. It is motivated by the need of methodologies and tools for the design of high-performance applications on dynamic reconfigurable computing systems. A complete methodology takes the reconfigurability of the hardware as an essential design concept and proposes the necessary mechanisms to fully exploit those capabilities at runtime. A set of tools must provide high-quality designs with improved designer productivity, which guarantees consistency with the initial requirements for adaptability and for the final implementation. This methodology allows designers to easily implement a system specification on a platform that includes general purpose processors dynamically combined with multiple accelerators running on an FPGA.

7.4. Collaboration with SME Ecreall

The transformation chain used in the DaRT Embedded System modeling approach involves several models automatically generated. This work aims to be able to modify directly ones of the generated model, and let the modification be propagated in both direction to other models of the chain. Not all changes can be propagated, a part of this work will be to identify changes that can be propagated. This work is done in collaboration with Ecreall (http://www.ecreall.com/), a small company involved in developing web collaborative portals. The first step of the work was to align MDE practice of the company to the DaRT practice. A first transformation chain has been developed. It allows to model collaborative portals, transform it in intermediate models, and then generate the code for a targeted technology (dolmen). This work will reuse results from the Traceability.

7.5. Collaboration with Thales

Partners: ENSIETA, INRIA (DaRT), Thales

In order to increase productivity and thus decrease time to market, we propose to apply Model Driven Engineering (MDE) through the use of process components, which encapsulate the main activities of co-design processes. We consider that activities going from requirements analysis to implementation, whatever the chosen life-cycle, can be capitalized through process components. They are several formalisms to describe a process (e.g., BPML, CPR, SPEM). We propose a modified version of OMG's SPEM profile (Software Process Engineering Modeling) in order to implement a full MDE process.

We experiment our approach in a co-design process based on the use of the new MARTE profile and we intend to provide a tool that implements it in order to help engineers. In [73], we explain our approach applied to the development of Radio Frequency Transceiver. During our experimentation, we had to face some problems of metamodel formalization using tools. We have then proposed in [74] a framework to define more formalized metamodels. The next challenging issue concerns the identification of a way our co-design process can be adapted to the Gaspard2 framework for design exploration. This work is done in the context of a CIFRE PhD contract co-supervised by Joël Champeau from ENSIETA (Brest) and Jean-Luc Dekeyser.

7.6. Collaboration within the MEDEE research pole

Partners: Valeo, INRIA (DaRT), L2EP

MEDEE (stands for "Maîtrise énergétique des entrainements électriques" http://l2ep.univ-lille1.fr/medee/) is a research pole involving many well-known industrial and academic partners. This group aims to improve numerical simulations for electric engines. The recent propositions aim to convert it to a competitive cluster. The DaRT project is especially involved in the first operation in the MEDEE program about simulations of these electrical engines. In fact, due to the large computation volume needed to run FEM simulations, most of the tracks lead to the use of parallel computers to solve these problems always faster.

7.7. Collaboration with GPUTech and Valeo

Partners: INRIA (DaRT), L2EP, GPUTech, Valeo

With the generalization of the GPGPU Computing (General Purpose GPU), we plan to add a new target for our Gaspard2 Framework: producing optimized code for GPU. This task is partially financed by Valeo, who plan to run their simulations on GPU, and by GPUTech (http://www.gputech.com/) who will include their technology in the framework.

7.8. The ANR Prima-Care project

Smail Niar is the scientific responsible of this project (http://www.primacare-project.com/). This one covers road crash prevention by the association of Intelligent Multi-sensor and radar, with dynamic management of sound alarms according to risk. Labeled by the cluster" iTrans.

7.9. The ANR Open-People project

Partners: Université de Bretagne Sud (UBS)Lab-STICC, INRIA Nancy Grand Est, INRIA Lille Nord Europe, Université de Rennes 1 (UR1), Université de Nice Sophia Antipolis (UNSA), THALES Communications (Colombes), InPixal (Rennes)

The Open-PEOPLE (Open Power and Energy Optimization PLatform and Estimator project is a national project funded by the ANR (Agence Nationale de la Recherche), the French National Research Agency. The objective of Open-PEOPLE is to provide a platform for estimating and optimizing the power and energy consumptions. Users will be able to estimate the consumption of an application deployed on a hardware architecture chosen in a set of parametric reference architectures. The components used in the targeted architecture will be chosen in a library of hardware and software components. Some of these components will be parametric (such as reconfigurable processors or ASIP) to further enlarge the design space for exploration. The library will be extensible; users will have the possibility to add new components, according to the evolution of both applications and technology. Open-PEOPLE is definitely an open project. The software platform for conducting estimation and optimization, will be accessible through an Internet portal. This software platform will be coupled to an automated hardware platform for physical measurements. The measurements needed to build models for new components to be added in the library will be remotely controlled through the software platform. A library of benchmarks will be proposed, to help building models for new components and architectures.

7.10. The ANR FAMOUS project

Partners: DaRT team of INRIA Lille Nord Europe, INRIA Rhone Alpes, Université de Bretagne Sud, Université de Bourgogne, Sodius

FAMOUS is a research project with an immediate industrial impact. Actually, it will make reconfigurable systems design easier and faster. The obtained tool in this project is expected to be used by both companies designers and academic researchers, especially for modern applications system specific design as smart camera, image and video processing ..etc. FAMOUS tools will be based on well established standards in design community. In fact, modeling will start from very high abstraction level using an extended version of MARTE. Simulation and synthetizable models will be obtained by automatic model to model transformations, using MDE approach. These techniques will contribute to shorten drastically time-to-market. FAMOUS is a basic research project. In fact, most of partners are academic, and its main objective is to explore novel design methodologies and target modern embedded systems architectures.

Until now, there no academic or industrial tool able to generate automatically SW/HW code for dynamically reconfigurable systems on FPGAs. In the ANR FAMOUS project, we defined a complete design flow, based on MDE approach, to model and design such systems. This flow allows handling application, architecture, allocation and control/ verification models. It generates implementation and synthesis code for Xilinx reconfigurable FPGAs. Some new concepts are already defined, in Famous, to be added to MARTE profile. They extend, for instance, the capabilities of MARTE by allowing modeling several architectures (corresponding to configurations) in the same model.

7.11. ID-TLM

In the framework of the collaboration between ST Micorelectronics and the INRIA, we are developing a collaboration (DGE ID TLM-NANO 2012, allocation n°3573) called ID-TLM between the team of Laurent Maillet-Contoz at ST Microelectronics and the AOSTE and DaRT INRIA teams.

The goal is to explore the contributions of the model driven engineering to the modeling and analysis of transaction level (TLM) models of computation (MoC). This collaboration has started on december 2008 and will last 4 years.

8. Other Grants and Activities

8.1. ARC INRIA - Triade

Partners: Aoste, DaRT, Espresso.

The goal of this project is to use formal models with structuring programmatic constructs as means to translate programs and descriptions written in formalisms widely used in Embedded System and SoC design (http://www.irisa.fr/espresso/Triade). Triade also aims to provide a seamless flow of increasingly time-defined and time-accurate models, so as to progressively obtain the final mapped implementation through provably correct steps from the early description elements.

8.2. STIC INRIA - Tunisia program

We have been co-advising two PhD students and several Master students in collaboration with the team of Pr. Mohamed Abid at CES-ENIS in Sfax and Pr. Abderrazak JEMAI at INSAT in Tunis. This collaboration is supported by the STIC Inria-Tunisia program, which aims at promoting the design of metamodels, transformation tools and techniques for the implementation of reconfigurable systems-on-chip. The resulting co-design environment will be validated on embedded systems dedicated to security in automobile, and more specifically in the design of cruise control systems integrating anti-collision radars.

Several successful student exchanges have been realized since 2006 between DaRT, INSAT and CES-ENIS.

8.3. Euromed 3+3 INRIA program

A collaboration supported by the Euromed 3+3 program started in 2009. It permits to initiate especially collaboration with the University of Monastir (Tunisia) with the team of Pr. Rached Torki on network on chip (NoC) modeling, evaluation and implementation. A co-advised PhD thesis is started on these issues between DaRT and U. Monastir.

8.4. International initiatives

8.4.1. ECSI

The European Electronic Chips & Systems design Initiative Missions are to identify, develop and promote efficient methods for electronic system design, with particular regards to the needs of the System-on-Chip and to provide ECSI members with a competitive advantage in this domain for the benefit of the European industry.

Our team has been an ECSI member since 2004. Pierre Boulet is a member of the executive committee of ECSI and secretary of ECSI.

8.4.2. Collaboration with Algéria

A collaboration has started with the university of Oran, Algeria. This collaboration with Abou El Hassan and his team has been active since 2006. We are working together on scheduling and mapping algorithms for SoC. An Egide-Tassili project an d a STIC-Algeria have been proposed to strengthen this collaboration.

8.4.3. Collaboration with Spain

We initiate a collaboration with IUMA, University of Las Palmas (Spain) with Antonio Nunez. Some visits and student exchanges are scheduled for the next months. Our collaboration focuses on NoC simulation, verification and design. Euromed 3+3 is one of the projects supporting this work.

8.4.4. Collaboration with Colombia

We initiate a collaboration with the Universitad de los Andes in Bogota and more precisely the team of software engineering directed by Rubby Casallas. A master student David Mendez came in our team during 4.5 months for an internship. Furthermore, Anne Etien has gone one week in Bogota to visit the team and develop the collaboration around the themes of model driven engineering and evolution.

8.4.5. Collaboration with Belgium

We initiate two collaborations with the Université Libre de Bruxelles, one with the flemish part (VUB) and one with the French speaking part (ULB). The first one concerns a collaboration with the Software Languages Lab and more specifically, Dirk Deridder's team. It focuses on model transformations. Alexis Muller and Anne Etien have visited them. The second one concerns the BEAMS team and focuses on design exploration. This collaboration aims to interoperate our tool Gaspard with their tool Nessy (http://beams.ulb.ac.be/beams/research/projects/current/119.html). For this purpose, several working meetings have been organized with Nastassia Gumuchdjian, Frédéric Robert and Alienor Richard from ULB and several members of the team. Antonio Paolilo

8.4.6. Collaboration with England

- A new collaboration with the Sosym team of the University of York in England has started this year. Anne Etien visit Richard Paige's team during two months through a "Programme Explorateur". We are working together on model driven engineering, evolution and genericity.
- We got a grant from the LIFL to establish a collaboration with the University of Hertfordshire, where is developed SAC (Single Assignment C). SAC is a C-like language used to express parallelism in programs and then their tools can produce real code for different target including Cuda (NVidia Language for GPGPU). In this collaboration, we look forward to integrate their low level optimizations in our Gaspard2 framework and they are interested in our expertise in high level expression for parallelism. In this context, Wendell Rodrigues, PhD in the DaRT team is visiting Hertfordshire University for 2 months from October 15th to December 15th.

8.4.7. Marte user group

Pierre Boulet has initiated the creation of the MARTE Users' Group.

The MARTE Users' Group is a group of persons and institutions using, evaluating or developing tools for the Modeling and Analysis of Real Time and Embedded systems UML profile. This profile is a standard of the OMG but the MARTE Users' Group is independent of any organizations, including the OMG. It aims at providing a forum for discussing the usages of MARTE, identifying and disseminating the good practices of MARTE tools, influencing the standard and providing resources to MARTE users.

The first action of this group is to organize a workshop in 2010, the 1st Workshop on Model Based Engineering for Embedded Systems Design, March 12, 2010 - Dresden, Germany, in coordination with the DATE'2010 conference.

8.5. National initiatives

We are members of the ASR[4] and SoC-SiP GDRs (research groups from the CNRS).

We are members of the Action IDM: a transverse group gathering teams of the ASR, GPL[5] and I3[6] GDRs.

[4] http://asr.cnrs.fr/
[5] http://gdr-gpl.cnrs.fr/
[6] http://www.cnrs.fr/ins2i/

9. Dissemination

9.1. Animation of the scientific community

The DaRT team participated to the organization of Euromicro DSD and SEAA 2010. These two conferences on respectively embedded system and software engineering themes took place from the 1rst to 3rd September in Polytech Lille. They gathered around 240 participants. http://www.dsdconf.org

Pierre Boulet has been in the steering committee and the program committee of FDL since 2005. He was Chair of M-BED'2010, the 1st workshop on Model Based Engineering for Embedded System Design, co-located with DATE'2010, Dresden, Germany 12 March 2010, and co-program chair of FDL'2010, Southampton, UK, 14-16 September 2010, and PC member of DATE'2010, dMEMS 2010. He is in the program committee of the DATE'2010 conference. He has initiated the MARTE user group and is co-organizer of the first workshop on Model Based Engineering for Embedded Systems in 2010 (co-located with DATE'2010). He was in several in 3 PhD thesis and one Hdr committees in 2010 . He has been deputy director of the LIFL since January 2008.

Smail Niar was PC member of Journal of System Architectures (JSA, ELSEVIER), Transactions of HiPeac (journal), Embedded systems Journal, Euromicro DSD de 2008 à 2010, Workshop on Parallel Programming and Run-time Management Techniques for Many-core Architectures 2010 and IEEE International Conference on Telecommunications 2010, Special Track on Reconfigurable Computing for Telecommunications, Networking, and Signal Processing, ICT2010. He is the scientific responsible of the mobile and embedded team of LAMIH at university of valenciennes.

Jean-Luc Dekeyser was in the program committee of the following conferences and workshops: DSD'2010, SoC'2010, AICCSA'2010, ReCoSoC'2010, IDT'2010, SYMPA2011, He was Chair of HOPES 2010. He has invited speaker in FETCH'2010 . He was in several PhD thesis and HdR committees in 2010. As director of the Ph.D. program at LIFL and Doctoral School SPI, he was involved in the belgium/france relationship concerning PhD program EuroDocInfo2010.

Anne Etien was member of the program committee of ECMFA 2010, the Model and Evolution Workshop organized jointly to the Models conference. She was also member of the PC of the French journal ISI for the special issue on Model driven engineering and traceability.

Cedric Dumoulin was member of the Program committee IDM10 9 - 12 March 2010, Pau (http://cal-idm-lmo-gpl-2010.univ-pau.fr/), Invited speaker "cup of science", Plateau Euratechnologies, 6 may 2010 and at the 'journee IDM 2010 a Lille', 2 December 2010, Lille (http://idm2010.lifl.fr/), Lille and finally he was Co-organizer of the 'journee IDM 2010 a Lille', 2 december 2010, Lille (http://idm2010.lifl.

Abdoulaye Gamatié is in the program committee of the Emsoft'2010, M-BED2010 and LCTES'2011 conferences. He is also organizing local chair of the DSD'2010 and SEAA'2010 conferences. He is member of a PhD thesis committee in 2010. Finally, he is member of the selection committee for PhD candidates and Post-doctorates at INRIA Lille - Nord Europe in 2010.

Frédéric Guyomarc'h is member of the program committee of PMAA'10.

Laure Gonnord is co-animator of the French compilation community : design and administration and the web site, member of the scientific staff. She was co-organizer (with F. Rastello) of the first compilation day in ÉNS Lyon (July 2010, Lyon, http://compilation.gforge.inria.fr)

9.2. Conference organisation

9.2.1. DSD and SEAA conferences

The full team participates to the organization of Euromicro DSD and SEAA 2010 (http://www.dsdconf.org/). These two conferences on respectively embedded system and software engineering themes took place from the 1rst to 3rd September in Polytech Lille. They gathered around 240 participants.

9.2.2. M-BED 2010 DATE friday workshop

We chaired the 1st workshop on Model Based Engineering for Embedded System Design, co-located with DATE'2010, Dresden, Germany 12 March 2010.

9.2.3. HOPES2010 ECMFA workshop

J-L Dekeyser was co-organizer of the First Workshop on Hands-on Platforms and tools for model-based engineering of Embedded Systems, Paris, France, June 15, in conjunction with ECMFA 2010.(http://www.ecmfa-2010.org/index.php/workshops/22)

9.2.4. MDE day

We co-organized in Montpellier the day on model driven engineering and evolution as a working day of the GPL GDR.

9.2.5. SoC Modeling day

We organized in Paris the one day seminary on "la Modelisation des SOC-SIP" as a SoC-SiP/ISIS GDR event.

9.2.6. RAPIDO Workshop

Smail Niar was co-organizer of the Rapid Simulation and Performance Evaluation: Methods and Tools " Rapido " sponsored by the European excellence network Hipeac , 2010 (Pise Italie), http://www2.lifl.fr/rapido09/Rapido/.

9.3. Teaching

As the DaRT team is mostly composed of professors and associate professors, we have a very large teaching activity. The more directly related to the research themes of the team was the master-level courses "System-on-Chip design" (Pierre Boulet, Jean-Luc Dekeyser, Samy Meftali, Abdoulaye Gamatié, Anne Etien), "Introduction to real-time operating systems" (Philippe Marquet), "Simulation of Systems and Architectures" (Philippe Marquet and Samy Meftali), "Distributed Systems and Infrastructures" (Pierre Boulet), "Advanced Computer Architecture" (Jean-Luc Dekeyser, Pierre Boulet, Calin Glitia), "SEMBA: Embedded system" (Abdoulaye Gamatié, Anne Etien, Rosilde Corvino, Thomas Legrand, Alexis Muller) and "Model Driven Engineering" (Anne Etien) and "Basics of Compilation" (Laure Gonnord). Cedric Dumoulin is responsible of a course on Advanced Object Conception, and another on New Technologies for the Web.

Smail Niar is in charge of several courses for master students in relationship of embedded system design, particularly "introduction to embedded system design" and "hardware/software co-design for high performance embedded systems". He was invited speaker to École thématique ECOFAC-CNRS 2010.

The following internships were advised in the team:

- David Mendez Universitad de los Andes, Bogota, Colombia, Transformation migration after meta-model evolution
- Mohamed Akli Redjedal, Université de Lille 1, master, multi-objective mapping and scheduling problem
- Antonio Paolillo, Université Libre de Bruxelles, Belgium, exploration implementation in Gaspard2
- Lacramioara Astefanoaiei , Centrum Wiskunde en Informatica Amsterdam ,July-September, verification techniques for rewriting-logic specifications.
- Abir Mastouri, PhD Student Sfax Tunisia, June-July - Scheduling in dynamically reconfigurable FPGAs

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