Activity Report 2015

Team CORSE

Compiler Optimization and Run-time SystEms

Inria teams are typically groups of researchers working on the definition of a common project, and objectives, with the goal to arrive at the creation of a project-team. Such project-teams may include other partners (universities or research institutions).

RESEARCH CENTER
Grenoble - Rhône-Alpes

THEME
Architecture, Languages and Compilation

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Team CORSE

Creation of the Team: 2014 November 01

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CORSE *is located at Giant/Minatec in Grenoble.*

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2. Overall Objectives

2.1. Overall Objectives

Languages, compilers, and run-time systems are some of the most important components to bridge the gap between applications and hardware. With the continuous increasing power of computers, expectations are evolving, with more and more ambitious, *computational intensive and complex applications*. As desktop PCs are becoming a niche and servers mainstream, three categories of computing impose themselves for the next decade: mobile, cloud, and super-computing. Thus *diversity, heterogeneity* (even on a single chip) and thus also *hardware virtualization* is putting more and more pressure both on compilers and run-time systems. However,

because of the energy wall, *architectures* are becoming more and more *complex* and *parallelism ubiquitous* at every level. Unfortunately, the memory-CPU gap continues to increase and energy consumption remains an important issue for future platforms. To address the challenge of *performance and energy consumption* raised by silicon companies, compilers and run-time systems must *evolve* and, in particular, interact, *taking into account the complexity of the target architecture*.

The overall objective of CORSE is to address this challenge by *combining static and dynamic compilation* techniques, with more interactive *embedding of programs and compiler environment in the runtime system*.

3. Research Program

3.1. Scientific Foundations

One of the characteristics of CORSE is to base our researches on diverse advanced mathematical tools. Compiler optimization requires the usage of the several tools around discrete mathematics: combinatorial optimization, algorithmic, and graph theory. The aim of CORSE is to tackle optimization not only for regular but also for irregular applications. We believe that new challenges in compiler technology design and in particular for split compilation should also take advantage of graph labeling techniques. In addition to runtime and compiler techniques for program instrumentation, hybrid analysis and compilation advances will be mainly based on polynomial and linear algebra.

The other specificity of CORSE is to address technical challenges related to compiler technology, runtime systems, and hardware characteristics. This implies mastering the details of each. This is especially important as any optimization is based on a reasonably accurate model. Compiler expertise will be used in modeling applications (e.g. through automatic analysis of memory and computational complexity); Runtime expertise will be used in modeling the concurrent activities and overhead due to contention (including memory management); Hardware expertise will be extensively used in modeling physical resources and hardware mechanisms (including synchronization, pipelines, etc.).

The core foundation of the team is related to the combination of static and dynamic techniques, of compilation, and runtime systems. We believe this to be essential in addressing high-performance and low energy challenges in the context of new important changes shown by current application, software, and architecture trends.

Our project is structured along two main directions. The first direction belongs to the area of runtime systems with the objective of developing strong relations with compilers. The second direction belongs to the area of compiler analysis and optimization with the objective of combining dynamic analysis and optimization with static techniques. The aim of CORSE is to ground those two research activities on the development of the end-to-end optimization of some specific domain applications.

4. Application Domains

4.1. Transfer

The main industrial sector related to the research activities of CORSE is the one of semi-conductor (programmable architectures spanning from embedded systems to servers). Obviously any computing application which has the objective of exploiting as much as possible the resources (in terms of high-performance but also low energy consumption) of the host architecture is intended to take advantage of advances in compiler and runtime technology. These applications are based over numerical kernels (linear algebra, FFT, convolution...) that can be adapted on a large spectrum of architectures. Members of CORSE already maintain fruitful and strong collaborations with several companies such as STMicroelectronics, Bull, Kalray, or Aselta.

Applying our techniques to a specific real application domain is cherished by all members of the team. In particular we believe (multi-scale) computational mechanics (such as fluid mechanics, molecular dynamics) to be a challenging domain that could take advantage both of compiler and run-time technologies that we intend to develop in CORSE. The goal is to provide an end-to-end solution to the automatic optimization (thus targeting portability of optimized code) of a specific application that requires extensive computational power. If we succeed our research should contribute indirectly to advances in that domain. We are still in the process of prospecting for the most appropriate application.

5. New Software and Platforms

5.1. Tirex

TIREX is an extensible, textual intermediate code representation that is intended to be used as an exchange format for compilers and other tools working on low level code. In the scope of the TIREX project we have developed tools for generating TIREX code from higher level languages such as C, as well as a number of static analyses and transformations.

Work on the TIREX project consisted of two main parts, firstly the cleanup and maintenance of the existing tools and web site and, secondly, implementing new backends for emitting TIREX.

The existing TIREX transormation and analysis tools as well the web site have been updated to make sure they work with the newest versions of their respective platforms (Java and PHP). They have also been refactored to make better use of newer or safer APIs. This work also included a redesign of the web site of the TIREX project and a rewrite of the build system.

The existing Open64 based backend has been updated to comply with the TIREX v2 specification so its output can be used with the rest of the tool chain.

We have also developed two new backends allowing us to generate TIREX code from any language the LLVM frontends support (including C, C++ and LLVM IR) as well as directly from assembly code. Preliminary work for generating TIREX directly from binaries has also been done, and the assembly backend is designed to allow most of its code to be reused for this purpose. These new developments required a partial rewrite of LLVMs internal machine description system to expose more machine information in an easily accessible manner. As a positive side effect we were able to reuse several parts used in earlier stages of the LLVM pipeline to write a simple type analysis on machine code used in the assembly backend. We also implemented a control flow reconstruction pass in the assembly backend to improve the quality of the generated code.

Lastly we have adopted continuous integration and started curating a regression test suite for our new developments.

5.2. LLVM plugins

Work has been started on multiple plugins for the LLVM compiler framework that implement the code optimization that have been elaborated by the team. While being work in progress this already provides us with crucial information for program analysis such as data-dependencies.

- Polly pointer disambiguation (publicly available): Status: Published. Description: A llvm-Polly patch that generates versioned SCoP, where the optimized version is guarded by run-time tests to validate that there are no hazardous aliasing.
- More on pointer disambiguation (to STMicroelectronics): Status: Implemented. Allows the use of malloc identifiers to quickly evaluate possible aliasing at run-time.
- Dynamic-dependence graph (to STMicroelectronics): Status: Under development. The run-time process is close to completion. Requires to treat function calls as sub-loops to allow optimization of recursive functions. The static analysis is capable of reading the trace file. The next step is to use a memory model to identify code transformations that would have better memory locality.

5.3. The klang-omp OpenMP compiler

Klang-Omp is a C and C++ source-to-source OpenMP compiler based on LLVM framework and on Intel's Clang-OMP front-end. It translates OpenMP directives into calls to task-based runtime system APIs. Klang-Omp currently targets both the StarPU runtime and the Kaapi runtime. The compiler supports independent tasks as defined by the 3.1 revision of the OpenMP specification as well as dependent tasks introduced with OpenMP 4. It also has been extended to support the omp target construct, making OpenMP applications able to offload computation to accelerators. This support also relies on the StarPU and XKaapi accelerator support capabilities. This work has been funded by the KSTAR Inria ADT project, involving the AVALON, STORM, MOAIS and CORSE Inria team. While the KSTAR project will end in January 2016, the klang-omp compiler will still be maintained and extended to support future OpenMP-oriented research actions, such as the ones promoted by the HEAVEN Persyval project.

5.4. mcGDB: Debugging of Multithreaded Applications

mcGDB is a new debugger for multithreaded applications. It implements a novel approach for interactive debugging named Programming Model-Centric Debugging. mcGDB raises interactive debugging to the level of programming models, by capturing and interpreting events generated during the application execution (e.g. through breakpointed API function calls). This new approach debugging is applied to four different programming models: software components (ST/NPM), Data flow (ST/PEDF), OpenCL and OpenMP. MCGDB was initialy developped by Kevin Pouget with STMicromectronics (CIFRE thesis). mcGDG uses the Temanejo graphical interface to display task graphs. mcGDB is currently extended in the DEMA/Nano2017 project with ST Microelectronics, Inria/Parkas and UPMC.

5.5. BOAST: Metaprogramming of Computing Kernels

BOAST aims at providing a framework to metaprogram, benchmark and validate computing kernels. BOAST is a programming framework dedicated to code generation and autotuning. This software allows the transformation from code written in the BOAST DSL to classical HPC targets like FORTRAN, C, OpenMP, OpenCL or CUDA. It also enables the meta-programming of optimization that can be (de)activated when needed. BOAST can also benchmark and do non regression tests on the generated kernels. This approach gives, both, performance gains and improved performance portability.

BOAST was used to generate and optimize the computing kernels of two scientific applications:

- BigDFT
- SPECFEM

BOAST can be dowloaded at this address https://forge.imag.fr/projects/boast/.

6. New Results

6.1. An interval constrained memory allocator for the Givy GAS runtime

Participants: François Gindraud, Fabrice Rastello, Albert Cohen [ENS Ulm], Francois Broquedis.

This work presents a memory allocator for a global address space (GAS) execution environment targeting manycore architectures with distributed memory. Among the family of Multi Processor System on Chip (MPSoC), these devices are composed of multiple nodes linked by an on-chip network; most nodes have multiple processors sharing a small local memory. An MPSoC has an excellent performance-per-Watt ratio, but it is hard to program due to multilevel parallelism, explicit resource and memory management, and hardware constraints (limited memory, network topology).

Practical programming frameworks let the programmer in charge of the hard, target-specific work (e.g., threads or node-local OpenMP plus explicit communications). Automatic, more abstract frameworks exist for specific (scientific) applications, but they target big systems and do not model the hardware constraints of MPSoC. Givy is a runtime system to execute dynamic task graphs on MPSoC. It has a focus on supporting irregular applications, and uses data-flow semantics to coordinate dynamic task scheduling and data transfer. To simplify the programmer's view of memory, both runtime and program data objects live in a GAS. To avoid address collisions when objects are dynamically allocated, and to maintain the consistency of these addresses across explicit data transfers and virtual memory remapping, a GAS-aware memory allocator is required. The allocator proposed in this work has the following properties: (1) it is free of inter-node synchronizations; (2) it is well suited for small memory systems; (3) its performances match that of existing state-of-the-art allocators.

6.2. On Characterizing the Data Access Complexity (IO) of Programs and Using it for Architectural Design Exploration

Participants: Venmugil Elango [OSU], Naser Sedaghati [OSU], Fabrice Rastello, Louis-Noël Pouchet [UCLA], J. Ramanujam [LSU], Radu Teodorescu [OSU], P. Sadayappan [OSU].

Technology trends will cause data movement to account for the majority of energy expenditure and execution time on emerging computers. Therefore, computational complexity will no longer be a sufficient metric for comparing algorithms, and a fundamental characterization of data access complexity will be increasingly important. The problem of developing lower bounds for data access complexity has been modeled using the formalism of Hong & Kung's red/blue pebble game for computational directed acyclic graphs (CDAGs). However, previously developed approaches to lower bounds analysis for the red/blue pebble game are very limited in effectiveness when applied to CDAGs of real programs, with computations comprised of multiple sub-computations with differing DAG structure. We address this problem by developing an approach for effectively composing lower bounds based on graph decomposition. We also develop a static analysis algorithm to derive the asymptotic data-access lower bounds of programs, as a function of the problem size and cache size.

The roofline model is a popular approach to "bounds and bottleneck" performance analysis. It focuses on the limits to performance of processors because of limited bandwidth to off-chip memory. It models upper bounds on performance as a function of operational intensity, the ratio of computational operations per byte of data moved from/to memory. While operational intensity can be directly measured for a specific implementation of an algorithm on a particular target platform, it is of interest to obtain broader insights on bottlenecks, where various semantically equivalent implementations of an algorithm are considered, along with analysis for variations in architectural parameters. This is currently very cumbersome and requires performance modeling and analysis of many variants.

We alleviate this problem by using the roofline model in conjunction with upper bounds on the operational intensity of computations as a function of cache capacity, derived using lower bounds on data movement. This enables bottleneck analysis that holds across all dependence-preserving semantically equivalent implementations of an algorithm. We demonstrate the utility of the approach in in assessing fundamental limits to performance and energy efficiency for several benchmark algorithms across a design space of architectural variations.

This work is the fruit of the collaboration 8.4 with OSU. The first contribution (static analysis for lower bound) will be presented at ACM POPL'15 [10]. The second contribution (architectural exploration) is to be published at ACM TACO'15 [3].

6.3. A Tiling Perspective for Register Optimization

Participants: Duco Van Amstel, Lukasz Domagala, P. Sadayappan [OSU], Fabrice Rastello.

Register allocation is a much studied problem. A particularly important context for optimizing register allocation is within loops, since a significant fraction of the execution time of programs is often inside loop code. A variety of algorithms have been proposed in the past for register allocation, but the complexity of the problem has resulted in a decoupling of several important aspects, including loop unrolling, register promotion, and instruction reordering.

In this work, we develop an approach to register allocation and promotion in a unified optimization framework that simultaneously considers the impact of loop unrolling and instruction scheduling. This is done via a novel instruction tiling approach where instructions within a loop are represented along one dimension and innermost loop iterations along the other dimension. By exploiting the regularity along the loop dimension, and imposing essential dependence based constraints on intra-tile execution order, the problem of optimizing register pressure is cast in a constraint programming formalism. Experimental results are provided from thousands of innermost loops extracted from the SPEC benchmarks, demonstrating improvements over the current state-of-the-art.

This work is the fruit of both the collaboration 8.4 with OSU and with Kalray 7.1 7.2.

6.4. Hybrid Data Dependence Analysis for Loop Transformations

Participants: Diogo Nunes Sampaio, Alain Ketterlin, Fabrice Rastello, Fernando Pereira, Alexandros Labrineas, Péricles Alves, Fabian Gruber.

Loop optimizations such as tiling, vectorization, or parallel task extraction are extremely important to achieve high performance. All such transformations rely on accurate memory dependence information to assess their validity. There are many practical situations, though, where dependence analysis fails to provide precise enough information. In this common scenario, the compiler will conservatively choose not to do any transformation. This happens in particular with low-level IRs (which are more and more common to address performance portability), but also in legacy code with pointers (e.g. C), linearized arrays, etc.

This work addresses the important problem of may-dependence disambiguation through the angle of a combination of static and dynamic analyses (sometimes called a hybrid analysis), similarly to what is already implemented in mainstream compilers, such as GCC, for auto-vectorization. This technique consists of adding a run-time test to disambiguate may-dependencies which static dependence analysis was not able to rule out. We propose two contributions to address this important problem.

The first approach proposes hybrid may-alias disambiguation. It combines two approaches: one that statically computes a symbolic expression of the interval of memory values a pointer may point to and uses dynamic overlap tests on these intervals to prove non-aliasing for each pair of pointers; another that hooks the memory allocator to find the base-pointer of a pointer and thus determine dynamically if a pointer pair belongs to two different allocations (and is thus disjoint) or not. We have applied these ideas on Polly-LLVM, a loop optimizer built on top of the LLVM compilation infrastructure. Our experiments indicate that our method is precise, effective and useful: we can disambiguate every pair of pointer in the loop intensive Polybench benchmark suite. The result of this precision is code quality: the binaries that we generate are 10% faster than those that Polly-LLVM produces without our optimization, at the -O3 optimization level of LLVM.

The second technique extends the non-overlapping intervals approach to may-dependence disambiguation. For this purpose, a powerful quantifier elimination scheme on multivariate-polynomials over integers has been developed. The quality of the presented scheme is important to make this approach realistic. In particular it must be precise (the integer aspect makes this problem very challenging), so that the test succeeds in practical cases, and must lead to negligible overhead. We evaluate preciseness and overhead on a set of 30+ benchmarks using complex loop transformations including loop fusion, skewing, and tiling.

This work is the fruit of the collaboration with UFMG 8.4, Kalray 7.1 7.2, STMicroelectronics 7.2, and with EPI CAMUS in the context of IPL Multicore 8.2. The first contribution has been presented at ACM OOPSLA'15 [19]. The second has been submitted to PLDI'16.

6.5. Power Efficiency and Computing Performance

Participants: Emilio Francesquini [UNICAMP, Campinas, Brazil], Edson Luiz Padoin [PhD: UFRGS and UNIJUI, Brazil], Marcio Castro [UFSC, Florianapolis, Brazil], Pedro Penna [PUC Minas, Belo Horizonte, Brazil], Henrique Cota de Freitas [PUC Minas, Belo Horizonte, Brazil], Fabrice Dupros [BRGM, Orléans, France], Philippe Navaux [UFRGS, Porto Alegre, Brazil], Jean François Méhaut.

Until the last decade, performance of HPC architectures has been almost exclusively quantified by their processing power. However, energy efficiency is being recently considered as important as raw performance and has become a critical aspect to the development of scalable systems. These strict energy constraints guided the development of a new class of so-called light-weight manycore processors. This study evaluates the computing and energy performance of two well-known irregular NP-hard problems – the Traveling-Salesman Problem (TSP) and K-Means clustering – and a numerical seismic wave propagation simulation kernel – Ondes3D – on multicore, NUMA, and manycore platforms. First, we concentrate on the nontrivial task of adapting these applications to a manycore, specifically the Kalray/MPPA-256 manycore processor. Then, we analyze their performance and energy consumption on those different machines. Our results show that applications able to fully use the resources of a manycore can have better performance and may consume from 3.8 × to 13 × less energy when compared to low-power and general-purpose multicore processors, respectively.

This work is the fruit of collaborations with Brazil and several universities (UFRGS, UFSC, UNICAMP, PUC Minas, USP). This work has been published in the journal of parallel and distributed computing [6] and in the journal of IET Computers and Digtal Techniques [7]. This work was also part of several international projects (LICIA, CNPq/Inria HOSCAR project, Exase).

Emilio Francesquini and Marcio Castro are also former PhD students of University Grenoble Alpes (UGA) and the LIG Laboratory.

6.6. Modeling and Simulating of Dynamic Task-Based Runtime Systems

Participants: Luka Stanisic [PhD, Inria, Mescal], Samuel Thibault [Univ. Bordeaux, Inria, Storm], Brice Videau, Arnaud Legrand [CNRS, Inria, Mescal], Jean François Méhaut.

Multi-core architectures comprising several GPUs have become mainstream in the field of High-Performance Computing. However, obtaining the maximum performance of such heterogeneous machines is challenging as it requires to carefully offload computations and manage data movements between the different processing units. The most promising and successful approaches so far build on task-based runtimes that abstract the machine and rely on opportunistic scheduling algorithms. As a consequence, the problem gets shifted to choosing the task granularity, task graph structure, and optimizing the scheduling strategies. Trying different combinations of these different alternatives is also itself a challenge. Indeed, getting accurate measurements requires reserving the target system for the whole duration of experiments. Furthermore, observations are limited to the few available systems at hand and may be difficult to generalize. In this work, we show how we crafted a coarse-grain hybrid simulation/emulation of StarPU, a dynamic runtime for hybrid architectures, over SimGrid, a versatile simulator for distributed systems. This approach allows to obtain performance predictions of classical dense linear algebra kernels accurate within a few percents and in a matter of seconds, which allows both runtime and application designers to quickly decide which optimization to enable or whether it is worth investing in higher-end GPUs or not. Additionally, it allows to conduct robust and extensive scheduling studies in a controlled environment whose characteristics are very close to real platforms while having reproducible behavior.

This work is part of the Luka Stanisic's thesis. Luka stanisic was coadvised by Arnaud Legrand, Brice Videau and Jean-François Méhaut. This thesis was defended in November 2015. Luka Stanisic currently holds a postdoc position at Inria Bordeaux in the Storm and HiePacs teams. This work was published in the CCPE journal [9].

6.7. Fast and Accurate Simulation of Multithreaded Sparse Linear Algebra Solvers

Participants: Luka Stanisic [PhD, Inria, Mescal], Arnaud Legrand [CNRS, Inria, Mescal], Emmanuel Agullo [Inria, HiePacs], Alfredo Buttari [CNRS, IRIT, Toulouse], Florent Lopez [CNRS, IRIT, Toulouse], Brice Videau.

The ever growing complexity and scale of parallel architectures imposes to rewrite classical monolithic HPC scientific applications and libraries as their portability and performance optimization only comes at a prohibitive cost. There is thus a recent and general trend in using instead a modular approach where numerical algorithms are written at a high level independently of the hardware architecture as Directed Acyclic Graphs (DAG) of tasks. A task-based runtime system then dynamically schedules the resulting DAG on the different computing resources, automatically taking care of data movement and taking into account the possible speed heterogeneity and variability. Evaluating the performance of such complex and dynamic systems is extremely challenging especially for irregular codes. In this article, we explain how we crafted a faithful simulation, both in terms of performance and memory usage, of the behavior of qr_mumps , a fully-featured sparse linear algebra library, on multi-core architectures. In our approach, the target high-end machines are calibrated only once to derive sound performance models. These models can then be used at will to quickly predict and study in a reproducible way the performance of such irregular and resource-demanding applications using solely a commodity laptop.

This work is part of the Luka Stanisic's thesis. Luka stanisic was coadvised by Arnaud Legrand, Brice Videau and Jean-François Méhaut. This thesis was defended in November 2015. Luka Stanisic currently holds a postdoc position at Inria Bordeaux in the Storm and HiePacs teams. This work was published in the ICPADS'2015 conference [18].

6.8. OpenMP Loop Scheduling

Participants: Pedro Penna [Master, PUC Minas, UFSC], Marcio Castro [Professor, UFSC], Henrique Cota de Freitas [Professor, PUC Minas], Francois Broquedis, Jean François Méhaut.

In High Performance Computing, the application's workload must be well balanced among the threads to achieve better performance. In this work, we propose a methodology that enables the design and exploration of new loop scheduling strategies. In this methodology, a simulator is used to evaluate the most relevant existing scheduling strategies, and a genetic algorithm is employed to explore the solution space of the problem itself. The proposed methodology allowed us to design a new loop scheduling strategy, which showed to be up to 32.3x better than the existing policies in terms of load balance.

6.9. BOAST: a Metaprogramming framework for computing kernels

Participants: Brice Videau [Postdoc CNRS, Mont-Blanc], Kevin Pouget [UJF, Nano2017], Luigi Genovese [Researcher, CEA INAC], Thierry Deutsch [Researcher, CEA INAC], Anthony Leonard [CNRS, Polytech Grenoble, Internship, from May 2015 until Aug 2015], Frederic Desprez, Jean François Méhaut.

Porting and tuning HPC applications to new platforms is tedious and costly in terms of human resources. Nonetheless, it is a very important aspect of the Mont-Blanc project. Indeed, for the Mont-Blanc project, more than ten applications were selected to be ported and optimized for the prototype platform.

Unfortunately, portability efforts are often lost when migrating to a new architecture. Worse, code may lose maintainability because several versions of some functionalities coexist, usually with a lot of duplication. Thus productivity of porting and tuning efforts is low as a huge fraction of those developments are never used after the platform they were intended for is decommissioned. Genericity of HPC codes is often limited. One of the reason is that producing generic code in Fortran 90/95 is difficult as the language does not really fit for it. Sometimes, adding genericity degrades performance as optimization opportunities that come from over-specification are lost. Functionality of HPC codes is tied to the previous point. Without genericity, adding new functionalities can be quite costly.

BOAST is a metaprogramming framework to produce portable and efficient computing kernels for HPC application. BOAST offers an embedded domain specific language to describe the kernels and their possible optimization. BOAST also supplies a complete runtime to compile, run, benchmark, and check the validity of the generated kernels. BOAST is being used in two flagship HPC applications BigDFT and SPECFEM3D, to improve performance portability of those codes.

BOAST is developped in the context of Mont-Blanc projects. It will be also used in the C2S@Exa IPL and the H2020/HPC4E project.

6.10. Performance comparison between Java and JNI for optimal implementation of computational micro-kernels

Participants: Nassim Halli [PhD student, CIFRE Aselta Nanographics], Henri-Pierre Charles [CEA LIST, CRI PILSI], Jean François Méhaut.

General purpose CPUs used in high performance computing (HPC) support a vector instruction set and an out-of-order engine dedicated to increase the instruction level parallelism. Hence, related optimizations are currently critical to improve the performance of applications requiring numerical computation. Moreover, the use of a Java run-time environment such as the HotSpot Java Virtual Machine (JVM) in high performance computing is a promising alternative. It benefits from its programming flexibility, productivity and the performance is ensured by the Just-In-Time (JIT) compiler. Though, the JIT compiler suffers from two main drawbacks. First, the JIT is a black box for developers. We have no control over the generated code nor any feedback from its optimization phases like vectorization. Secondly, the time constraint narrows down the degree of optimization compared to static compilers like GCC or LLVM. So, it is compelling to use statically compiled code since it benefits from additional optimization reducing performance bottlenecks. Java enables to call native code from dynamic libraries through the Java Native Interface (JNI). Nevertheless, JNI methods are not inlined and require an additional cost to be invoked compared to Java ones. Therefore, to benefit from better static optimization, this call overhead must be leveraged by the amount of computation performed at each JNI invocation. In this work we tackle this problem and we propose to do this analysis for a set of micro-kernels. Our goal is to select the most efficient implementation considering the amount of computation defined by the calling context. We also investigate the impact on performance of several different optimization schemes which are vectorization, out-of-order optimization, data alignment, method inlining and the use of native memory for JNI methods.

This work was presented in the ADAPT'2015 workshop. It's alsop part of the Nassim Halli's thesis.

6.11. Reducing trace size in multimedia applications endurance tests

Participants: Serge Emteu [PhD ST Microelectronics, LIG/Slide, CORSE], Miguel Santana [ST Microelectrnics], Alexadre Termier [Prof. Univ. Rennes I, IRISA/Inria/Dream], René Quiniou [CR Inria, IRISA/Inria/Dream], Brice Videau [Postdoc CNRS, Inria/Corse], Jean François Méhaut.

The consumer electronics market is dominated by embedded systems due to their ever-increasing processing power and the large number of functionnalities they offer. To provide such features, architectures of embedded systems have increased in complexity : they rely on several heterogeneous processing units, and allow concurrent tasks execution. This complexity degrades the programmability of embedded system architectures and makes application execution difficult to understand on such systems. The most used approach for analyzing application execution on embedded systems consists in capturing execution traces (event sequences, such as system call invocations or context switch, generated during application execution). This approach is used in application testing, debugging or profiling. However in some use cases, execution traces generated can be very large, up to several hundreds of gigabytes. For example endurance tests, which are tests consisting in tracing execution of an application on an embedded system during long periods, from several hours to several days. Current tools and methods for analyzing execution traces are not designed to handle such amounts of data.

We propose an approach for monitoring an application execution by analyzing traces on the fly in order to reduce the volume of recorded traces. Our approach is based on features of multimedia applications which contribute the most to the success of popular devices such as set-top boxes or smartphones. This approach consists in identifying automatically the suspicious periods of an application execution in order to record only the parts of traces which correspond to these periods. The proposed approach consists of two steps : a learning step which discovers regular behaviors of an application from its execution trace, and an anomaly detection step which identifies behaviors deviating from the regular ones.

The many experiments, performed on synthetic and real-life datasets, show that our approach reduces the trace size by an order of magnitude while maintaining a good performance in detecting suspicious behaviors.

This work was presented at the DATE conference in Grenoble. It was also part of the Serge Emteu's thesis wth ST Microelectronics.

6.12. Data Mining Approach to Temporal Debugging of Embedded Streaming Applications

Participants: Oleg Iegorov [PhD ST Microelectronics, LIG/Slide, CORSE], Miguel Santana [ST Microelectrnics], Alexadre Termier [Prof. Univ. Rennes I, IRISA/Inria/Dream], Vincent Leroy [Associate Professor UJF, LIG/Slide], Jean François Méhaut.

One of the greatest challenges in the embedded systems area is to empower software developers with tools that speed up the debugging of QoS properties in applications. Typical streaming applications, such as multimedia (audio/video) decoding, fulfill the QoS properties by respecting the realtime deadlines. A perfectly functional application, when missing these deadlines, may lead to cracks in the sound or perceptible artifacts in the image.

We start from the premise that most of the streaming applications that run on embedded systems can be expressed under a dataflow model of computation, where the application is represented as a directed graph of the data flowing through computational units called actors. It has been shown that in order to meet real-time constraints the actors should be scheduled in a periodic manner. We exploit this property to propose SATM – a novel approach based on data mining techniques that automatically analyzes execution traces of streaming applications, and discovers significant breaks in the periodicity of actors, as well as potential causes of these breaks. We show on a real use case that our debugging approach can uncover important defects and pinpoint their location to the application developer.

This work was presented at the EMSOFT conference in Amsterdam. It was also part of the Oleg Iegorov's thesis wth ST Microelectronics.

6.13. Tiling Bitwise Computations Using Look-up Instructions

Participants: Florent Bouchez - Tichadou, Cyril Six [Inria, Internship, from Feb 2015 until Jun 2015].

The BWLU is an instruction of a Very Long Instruction Word processor (VLIW) that performs a series of bit-independent computations in only one step through the use of a "look-up table" (LUT). The Bit-Wise Look-Up table instruction (BWLU) takes as input four registers as well as a 32-bit integer (the "table"), and is able to output two bit-independent computations based on the input registers into two output registers.

The goal is to make the best use possible of this instruction by replacing during compilation as much as possible groups of bitwise computation using BWLUs so as to reduce the number of instructions required to perform a computation. The problem is represented by a data-flow graph representing a computation, and the goal is use BLWUs as tiles to "match" groups of bitwise instruction.

We proved the problem NP-complete for a general data-flow graph, so it is not practical to try to find the optimal solution.

It is easy to devise a greedy algorithm that will produce a solution, but we wanted a way to check whether the solutions found where far from the optimal. An optimal algorithm is of course exponential in the size of the input graph, however, we devised a complete space exploration algorithm based on dynamic programming that manages to find the optimal solution for data-flow graphs with small width or height.

7. Bilateral Contracts and Grants with Industry

7.1. Bilateral Contract with Industry

- Tirex is a bilateral contract with Kalray. The subject is a prototyping of hybrid alias analysis. The collaboration led to a recent publication which corresponding work is described in 6.4.

7.2. Bilateral Grants with Industry

- ManyCoreLabs is a bilateral Grant (BGLE) with Kalray. CORSE is involved in the development of generalized register tiling.
- PSAIC Nano2017 is a bilateral Grant with STMicroelectronics. CORSE is involved in the development of trace analysis and hybrid compilation.
- DEMA Nano2017 is a bilateral Grant with STMicroelectronics. CORSE is involved in the development of debugging of multithreaded applications.

7.3. CIFRE contracts

- CORSE is involved in another contract with Kalray associated with the CIFRE PhD of Duco van Amstel. The subject of the collaboration is related to fine grain scheduling. Corresponding work is described in 6.3.
- CORSE is involved in a contract with Aselta for the CIFRE thesis of Nassim Halli.
- CORSE is also involved in two contracts with STMicroelectronics for the CIFRE theses of Serge Emteu and Oleg Iegorov.

8. Partnerships and Cooperations

8.1. Regional Initiatives

8.1.1. HEAVEN Persyval Project

- Title: HEterogenous Architectures: Versatile Exploitation and programiNg
- HEAVEN leaders: François Broquedis, Olivier Muller[TIMA lab]
- Corse participants: François Broquedis, Frédéric Desprez, Georgios Christodoulis
- Computer architectures are getting more and more complex, exposing massive parallelism, hierarchically-organized memories and heterogeneous processing units. Such architectures are extremely difficult to program as they most of the time make application programmers choose between portability and performance.

  While standard programming environments like OpenMP are currently evolving to support the execution of applications on different kinds of processing units, such approaches suffer from two main issues. First, to exploit heterogeneous processing units from the application level, programmers need to explicitly deal with hardware-specific low-level mechanisms, such as the memory transfers between the host memory and private memories of a co-processor for example. Second, as the evolution of programming environments towards heterogeneous programming mainly focuses on CPU/GPU platforms, some hardware accelerators are still difficult to exploit from a general-purpose parallel application.

  FPGA is one of them. Unlike CPUs and GPUs, this hardware accelerator can be configured to fit the application needs. It contains arrays of programmable logic blocks that can be wired together to build a circuit specialized for the targeted application. For example, FPGAs can be configured to accelerate portions of code that are known to perform badly on CPUs or GPUs. The energy

efficiency of FPGAs is also one of the main assets of this kind of accelerators compared to GPUs, which encourages the scientific community to consider FPGAs as one of the building blocks of large scale low-power heterogeneous multicore platforms.

However, only a fraction of the community considers programming FPGAs for now, as configurations must be designed using low-level description languages such as VHDL that application programmers are not experienced with.

The main objective of this project is to improve the accessibility of heterogeneous architectures containing FPGA accelerators to parallel application programmers. The proposed project focuses on three main aspects:

- Portability: we don't want application programmers to redesign their applications completely to benefit from FPGA devices. This means extending standard parallel programming environments like OpenMP to support FPGA. Improving application portability also means leveraging most of the hardware-specific low-level mechanisms at the runtime system level ;
- Performance: we want our solution to be flexible enough to get the most out of any heterogeneous platforms containing FPGA devices depending on specific performance needs, like computation throughput or energy consumption for example ;
- Experiments: Experimenting with FPGA accelerators on real-life scientific applications is also a key element of our project proposal. In particular, the solutions developed in this project will allow comparisons between architectures on real-life applications from different domains like signal processing and computational finance.

Efficient programming and exploitation of heterogeneous architectures implies the development of methods and tools for system design, embedded or not. The HEAVEN project proposal fits in the PCS research action of the PERSYVAL-lab. The PhD of Georgios Christodoulis is funded by this project.

8.1.2. HPES Persyval Project

- Title: High Performance Embedded Systems
- HPES leader: Henri-Pierre Charles [CEA List, CRI PILSI]
- HPES participants: Suzane Lesecq [CEA Leti], Laurent Fesquet [TIMA Lab], Stéphane Mancini [TIMA Lab], Eric Ruten [Inria/CtrlA], Nicolas Marchand [Gipsa Lab], Bogdan Robu [Gipsa Lab]
- Corse participants: Naweiluo Zhou [PhD Persyval], Fabrice Rastello, Jean-François Méhaut
- The computing area has been recently deeply modified by the emergence of the so-called multicore processor. Within the same chip, several computing units are implemented. This architectural concept allows meeting the performance requirements under stringent energy consumption constraints. Multicores are used for laptops, Graphical Processor Units (GPU), High Performance Computing (HPC) platforms, but also for embedded systems su ch as mobile phones. Moreover, low-power high performance multicores developed for embedded systems will be soon used in data centers for HPC. This raises new scientific challenges to architecture, systems and application designers that have face massively parallel computing platforms.

  The number of cores on a chip is increasing quickly. At the same time, the memory bandwidth is increasing too slowly to ensure the performance such multicore platforms should attain. This phenomenon is known as "Memory Wall" and at the moment no efficient solution to exceed this limitation exists. With the increase in the number of cores, cache coherency is becoming as well a tremendous challenge.

  Power consumption is also a huge challenge as it imposes strong constraints on the computing platform, whatever the application domain. The first machine ranked in the Green500 has an energy performance ratio of 2 Gflops per watt. This ratio has to be improved by 30 when exascale computing is considered. The multi-core processor might help to improve this ratio; however, the software stack should as well evolve to boost this improvement.

8.2. National Initiatives

8.2.1. IPL Multicore

- Title: Large scale multicore virtualization for performance scaling and portability
- Multicore leader: Gilles Muller
- CORSE participants: Fabrice Rastello
- Multicore processors are becoming the norm in most computing systems. However supporting them in an efficient way is still a scientific challenge. This large-scale initiative introduces a novel approach based on virtualization and dynamicity, in order to mask hardware heterogeneity, and to let performance scale with the number and nature of cores. It aims to build collaborative virtualization mechanisms that achieve essential tasks related to parallel execution and data management. We want to unify the analysis and transformation processes of programs and accompanying data into one unique virtual machine. We hope delivering a solution for compute-intensive applications running on general-purpose standard computers. Research directions are: (1) Memory management and scheduling; (2) Garbage collection; (3) Improving data locality; (4) Dynamic parallelization; (5) Fast execution of Sequential Sections; (6) Dynamic Code Generation; (7) Dynamic Binary Rewriting for Performance Portability; (8) Virtualization of floating-point computation; (9) Convergence between VMKit and StarPU

8.2.2. IPL C2S@Exa

- Title: Computer and Computational Sciences at Exascale
- C2S@Exa leader: Stéphane Lanteri
- Corse participants: François Broquedis, Frédéric Desprez, Jean-François Méhaut
- The C2S@Exa Inria large-scale initiative is concerned with the development of numerical modeling methodologies that fully exploit the processing capabilities of modern massively parallel architectures in the context of a number of selected applications related to important scientific and technological challenges for the quality and the security of life in our society. At the current state of the art in technologies and methodologies, a multidisciplinary approach is required to overcome the challenges raised by the development of highly scalable numerical simulation software that can exploit computing platforms offering several hundreds of thousands of cores. Hence, the main objective of the C2S@Exa Inria large-scale initiative is the establishment of a continuum of expertise in the computer science and numerical mathematics domains, by gathering researchers from Inria project-teams whose research and development activities are tightly linked to high performance computing issues in these domains. More precisely, this collaborative effort involves computer scientists that are experts of programming models, environments and tools for harnessing massively parallel systems, algorithmists that propose algorithms and contribute to generic libraries and core solvers in order to take benefit from all the parallelism levels with the main goal of optimal scaling on very large numbers of computing entities and, numerical mathematicians that are studying numerical schemes and scalable solvers for systems of partial differential equations in view of the simulation of very large-scale problems.

8.2.3. PIA ELCI

- Title: Environnement logiciel pour le calcul intensif
- ELCI leader: Corinne Marchand (BULL SAS)
- Corse participants: François Broquedis, Philippe Virouleau
- Duration: from Sept. 2014 to Sept. 2017

- The ELCI project main goal is to develop a highly-scalable new software stack to tackle high-end supercomputers, from numerical solvers to programming environments and runtime systems. In particular, the CORSE team is studying the scalability of OpenMP runtime systems on large scale shared memory machines through the PhD of Philippe Virouleau, co-advised by researchers from the CORSE and AVALON Inria teams. This work intends to propose new approaches based on a compiler/runtime cooperation to improve the execution of scientific task-based programs on NUMA platforms. The PhD of Philippe Virouleau is funded by this project.

8.3. European Initiatives

8.3.1. FP7 & H2020 Projects

8.3.1.1. Mont-Blanc

Title: Mont-Blanc (European scalable and power efficient HPC platform based on low-power embedded technology)

Program FP7

Duration: 01/10/2011 - 30/06/2015

Coordinator: Barcelona Supercomputing Center (BSC)

Mont-Blanc consortium: BSC, Arm, Bull, CNRS, CEA Leti, Juelich, LRZ, Genci, Cineca, Univ. Cantabria

Mont-Blanc website: http://www.montblanc-project.eu/

Corse contact: Jean-François Méhaut

Corse participants: Brice Videau, Kevin Pouget

There is a continued need for higher compute performance: scientific grand challenges, engineering, geophysics, bioinformatics, etc. However, energy is increasingly becoming one of the most expensive resources and the dominant cost item for running a large supercomputing facility. In fact the total energy cost of a few years of operation can almost equal the cost of the hardware infrastructure. Energy efficiency is already a primary concern for the design of any computer system and it is unanimously recognized that Exascale systems will be strongly constrained by power. The analysis of the performance of HPC systems since 1993 shows exponential improvements at the rate of one order of magnitude every 3 years: One petaflops was achieved in 2008, one exaflops is expected in 2020. Based on a 20 MW power budget, this requires an efficiency of 50 GFLOPS/Watt. However, the current leader in energy efficiency achieves only 1.7 GFLOPS / Watt. Thus, a 30x improvement is required. In this project, we believe that HPC systems developed from today's energy-efficient solutions used in embedded and mobile devices are the most likely to succeed. As of today, the CPUs of these devices are mostly designed by ARM. However, ARM processors have not been designed for HPC, and ARM chips have never been used in HPC systems before, leading to a number of significant challenges. The Mont-Blanc project has three objectives:

- To develop a fully functional energy-efficient HPC prototype using low-power commercially available embedded technology
- To design a next-generation HPC system together with a range of embedded technologies in order to overcome the limitations identified in the prototype system
- To develop a portfolio of exascale applications to be run on this new generation of HPC systems. This will produce a new type of computer architecture capable of setting future global HPC standards that will provide Exascale performance using 15 to 30 times less energy

8.3.1.2. Mont-Blanc2

Title: Mont-Blanc (European scalable and power efficient HPC platform based on low-power embedded technology)

Program FP7

Duration: 01/10/2013 - 30/09/2016

Coordinator: Barcelona Supercomputing Center (BSC)

Mont-Blanc consortium: BSC, Bull, Arm, Juelich, LRZ, USTUTT, Cineca, CNRS, Inria, CEA Leti, Univ. Bristol, Allinea

Corse contact: Jean-François Méhaut

Corse participants: Brice Videau, Kevin Pouget

The Mont-Blanc project aims to develop a European Exascale approach leveraging on commodity power-efficient embedded technologies. The project has developed a HPC system software stack on ARM, and is deployed the first integrated ARM-based HPC prototype by 2014, and is also working on a set of 11 scientific applications to be ported and tuned to the prototype system.

The rapid progress of Mont-Blanc towards defining a scalable power efficient Exascale platform has revealed a number of challenges and opportunities to broaden the scope of investigations and developments. Particularly, the growing interest of the HPC community in accessing the Mont-Blanc platform calls for increased efforts to setup a production-ready environment. The Mont-Blanc 2 proposal has 4 objectives:

1. To complement the effort on the Mont-Blanc system software stack, with emphasis on programmer tools (debugger, performance analysis), system resiliency (from applications to architecture support), and ARM 64-bit support
2. To produce a first definition of the Mont-Blanc Exascale architecture, exploring different alternatives for the compute node (from low-power mobile sockets to special-purpose high-end ARM chips), and its implications on the rest of the system
3. To track the evolution of ARM-based systems, deploying small cluster systems to test new processors that were not available for the original Mont-Blanc prototype (both mobile processors and ARM server chips)
4. To provide continued support for the Mont-Blanc consortium, namely operations of the original Mont-Blanc prototype, the new developer kit clusters and hands-on support for our application developers

Mont-Blanc 2 contributes to the development of extreme scale energy-efficient platforms, with potential for Exascale computing, addressing the challenges of massive parallelism, heterogeneous computing, and resiliency. Mont-Blanc 2 has great potential to create new market opportunities for successful EU technology, by placing embedded architectures in servers and HPC.

8.3.1.3. HPC4E

Title: HPC for Energy

Programm: H2020

Duration: 01/12/2015 - 30/11/2017

Coordinator: Barcelona Supercomputing Center (BSC)

European partners: Inria, Univ. Lancaster, Ciemat, Total, Repsol, Iberdrola

Brazilian partners: Coppe, LNCC, ITA, Petrobras, UFRGS, UFPE

Inria contact: Stephane Lanteri

Corse contact: Jean-François Méhaut

Corse participants: François Broquedis, Frédéric Desprez, Brice Videau

The main objective is to develop beyond-the-state-of-the-art high performance simulation tools that can help the energy industry to respond future energy demands and also to carbon-related environmental issues using the state-of-the-art HPC systems. HPC4E also aims at improving the usage of energy using HPC tools by acting at many levels of the energy chain for different energy sources. The project includes relevant energy industral partners from Brazil and EU, which will benefit from the project's results. They guarantee that TRL of the project technologies will be very high.

8.3.1.4. EoCoE

Title: Energy oriented Centre of Excellence for computer applications

Programm: H2020

Duration: 01/10/2015 - 30/11/2018

Coordinator: Commissariat à L'Energie Atomique et aux Energies Alternatives (CEA)

European partners: CEA, Juelich, MPG, Enea, Cerfacs, UNITN, Fraunhofer, Univ. Bath, CNR, Univ. Brussels, BSC

Inria contact: Michel Kern

Corse contact: Jean-François Méhaut

Corse participants: François Broquedis, Frédéric Desprez, Brice Videau

This projects establishes an Energy Oriented Centre of Excellence for computing applications, (EoCoE). EoCoE (pronounce "Echo") will use the prodigious potential offered by the ever-growing computing infrastructure to foster and accelerate the European transition to a reliable and low carbon energy supply. To achieve this goal, we believe that the present revolution in hardware technology calls for a similar paradigm change in the way application codes are designed. EoCoE will assist the energy transition via targeted support to four renewable energy pillars: Meteo, Materials, Water and Fusion, each with a heavy reliance on numerical modelling. These four pillars will be anchored within a strong transversal multidisciplinary basis providing high-end expertise in applied mathematics and HPC. EoCoE is structured around a central Franco-German hub coordinating a pan-European network, gathering a total of 8 countries and 23 teams. Its partners are strongly engaged in both the HPC and energy fields; a prerequisite for the long-term sustainability of EoCoE and also ensuring that it is deeply integrated in the overall European strategy for HPC. The primary goal of EoCoE is to create a new, long lasting and sustainable community around computational energy science. At the same time, EoCoE is committed to deliver high-impact results within the first three years. It will resolve current bottlenecks in application codes, leading to new modelling capabilities and scientific advances among the four user communities; it will develop cutting-edge mathematical and numerical methods, and tools to foster the usage of Exascale computing. Dedicated services for laboratories and industries will be established to leverage this expertise and to foster an ecosystem around HPC for energy. EoCoE will give birth to new collaborations and working methods and will encourage widely spread best practices.

8.4. International Initiatives

8.4.1. Inria International Labs

- JLESC (Joint Laboratory on Exascale Computing)
  The CORSE team is involved in the JLESC with collaborations with UIUC (Sanjay Kalé) and BSC (Mont-Blanc projects). Kevin Pouget, Brice Videau and Jean-François Méhaut attended to the two JLESC workshops (Barcelona and Bonn) in 2015.
  - **Energy Efficiency and Load Balancing**
  - The power consumption of High Performance Computing (HPC) systems is an increasing concern as large-scale systems grow in size and, consequently, consume more energy. In response to this challenge, we propose new energy-aware load balancers that aim at reducing the energy consumption of parallel platforms running imbalanced scientific applications without degrading their performance. Our research explores dynamic load balancing, low power manycore platforms and DVFS techniques in order to reduce power consumption.

  - We propose the improvement of the performance and scalability of parallel seismic wave models through dynamic load balancing. These models suffer from load imbalance for two reasons. First, they add a specific numerical condition at the borders of the domain, in order to absorb the outgoing energy. The decomposition of the domain into a grid of subdomains, which are distributed among tasks, creates load differences between the tasks that simulate the borders and those responsible for the central subdomains. Second, the propagation of waves in the simulated area changes the workload on the subdomains on different time-steps. Therefore causing dynamic load imbalance. In order to evaluate the use of dynamic load balancing, we ported a seismic wave simulator to Adaptive MPI, to benefit from its load balancing framework. Our experimental results show that dynamic load balancers can adapt to load variations during the application's execution and improve performance by 36%.
  - we also focus on reducing the energy consumption of imbalanced applications through a combination of load balancing and Dynamic Voltage and Frequency Scaling (DVFS). Our strategy employs an Energy Daemon Tool to gather power information and a load balancing module that benefits from the load balancing framework available in the CHARM++ runtime system. We propose two variants of our energy-aware load balancer (ENERGYLB) to save energy on imbalanced workloads without considerably impacting the overall system performance. The first one, called Fine- Grained EnergyLB (FG-ENERGYLB), is suitable for plat- forms composed of few tens of cores that allow per-core DVFS. The second one, called Coarse-Grained EnergyLB (CG-ENERGLB) is suitable for current HPC platforms composed of several multi-core processors that feature per-chip DVFS.

- LIRIMA (IDASCO team)
  - The general objective of IDASCO project team is to develop models and tools that can be used to collect the huge amount of data produced by complex computational, biological, epidemiological or environmental systems, and extract knowledge from these data in order to better understand their structure and dynamics for decision making. From 2010 to 2015, the IDASCO activities were focused on the following main thematics : programming environments for parallel execution, parallel algorithms for datamining, social network analysis and trace mining. Some work on wireless sensor networks and geographic information systems with application to sustainable management of natural resources have also been developed. Ten PhD Theses were defended during this period with eight on them co-supervised. There were some industrial collaborations with a brewery company (SABC) on e-Learning platforms and with ORANGE Labs on online registration platforms. These collaborations were done in partnership of the ALOCO project team. The EPICAM project was also developed in partnership with MEDES France, Centre Pasteur Cameroun and the National Program for Fight against Tuberculosis.
  - Jean-François Méhaut is co-director with Maurice Tchuenté of the IDASCO team.
  - Thomas Messi Nguelé is currently preparing a PhD with the coadvising of Maurice Tchuenté. His research work is also part of the IDASCO team.
  - Ylies Falcone and Jean-François Méhaut spent two weeks in Cameroon (Yaoundé) in the context of LIRIMA and CETIC (African Center of Excellence for IT, http://www.cetic.cm/).

8.4.2. Inria Associate Teams not involved in an Inria International Labs

8.4.2.1. IOComplexity

Title: Automatic characterization of data movement complexity

International Partner (Institution - Laboratory - Researcher):

Ohio State University (United States) - P. Sadayappan

Start year: 2015

See also: https://team.inria.fr/corse/iocomplexity/

The goal of this project is to develop new techniques and tools for the automatic characterization of the data movement complexity of an application. The expected contributions are both theoretical and practical, with the ambition of providing a fully automated approach to I/O complexity characterization, in starking contrast with all known previous work that are stricly limited to pen-and-paper analysis.

I/O complexity becomes a critical factor due in large part to the increasing dominance of data movement over computation in energy consumption for current and emerging architectures. This project aims at enabling: 1. the selection of algorithms according to this new criteria (as opposed to the criteria on arithmetic complexity that has been used up to now); 2. the design of specific architectures in terms of cache size, memory bandwidth, GFlops etc. based on application-specific bounds on memory traffic; 3. higher quality feedback to the user, the compiler, or the run-time system about data traffic, a major performance and energy factor.

8.4.2.2. PROSPIEL

- Title: Profiling and specialization for locality
- International Partner (Institution - Laboratory - Researcher):

  Universidade Federal de Minas Gerais (Brazil) - Computer Science Department - Fernando Magno Quintão Pereira
- Start year: 2015
- See also: https://team.inria.fr/alf/prospiel/
- The PROSPIEL project aims at optimizing parallel applications for high performance on new throughput-oriented architectures: GPUs and many-core processors. Traditionally, code optimization is driven by a program analysis performed either statically at compile-time, or dynamically at run-time. Static program analysis is fully reliable but often over-conservative. Dynamic analysis provides more accurate data, but faces strong execution time constraints and does not provide any guarantee. By combining profiling-guided specialization of parallel programs with runtime checks for correctness, PROSPIEL seeks to capture the advantages of both static analysis and dynamic analysis. The project relies on the polytope model, a mathematical representation for parallel loops, as a theoretical foundation. It focuses on analyzing and optimizing performance aspects that become increasingly critical on modern parallel computer architectures: locality and regularity.

8.4.2.3. Exase

Title: Exascale Computing Scheduling Energy

See also: https://team.inria.fr/exase/

Inria leader: Jean-Marc Vincent (Mescal)

Inria teams: Mescal, Moais, Corse

Corse participants: Jean-François Méhaut, François Broquedis, Frédéric Desprez

International Partner (Institution - Laboratory - Researcher):

Federal University of Rio Grande do Soul (UFRGS, Porto Alegre, Brazil) - Informatics Faculty - L. Schnoor, N. Maillard, P. Navaux

Pontifical University Minas (PUC Minas, Belo Horizonte, Brazil) - Computer Science faculty, Henrique Freitas

University of Sao Paulo (USP, Sao Paulo, Brazil), IME faculty, Alfredo Goldman

Start year: 2014

The main scientific goal of Exase for the three years is the development of state-of- the-art energy-aware scheduling algorithms for exascale systems. As previously stated, issues on energy are fundamental for next generation parallel platforms and all scheduling decisions must be aware of that. Another goal is the development of trace analysis techniques for the behavior analysis of schedulers and the applications running on exascale machines. We list below specific objectives for each development axis presented in the previous section. analysis.

- Fundamentals for the scaling of schedulers
- Design of schedulers for large-scale infrastructures
- Tools for the analysys of large scale schedulers

8.4.3. Participation In other International Programs

- LICIA
- HOSCAR
- EnergySFE (STIC Amsud)

8.5. International Research Visitors

8.5.1. Visits of International Scientists

- Thierry Jéron, Hervé Marchand, and Antoine Rollet visited Yliès Falcone during 1 week in January 2015.
- Ezio Bartocci (TU Vienna) visited Y. Falcone during two weeks in August 2015.
- Sylvain Hallé (University of Québec at Chicoutimi) visited Yliès Falcone during 1 week in December 2015.

8.5.2. Visits to International Teams

8.5.2.1. Research stays abroad

- Fabrice Rastello visited P. Sadayappan at Ohio State University two times one month (mai 2015 + September 2015) in the context of the INRIA Associate Team IOComplexity.
- Ylies Falcone visited the University of Illinois at Urbana Champaign (USA) from February to July 2015.
- Jean-François Méhaut visited M. Tchuenté at Yaoundé. (February 2015) in the context of LIRIMA (Idasco team).
- Jean-François Méhaut visited P. Navaux at UFRGS (October 2015) in the context of LICIA and the Inria associated team Exase.
- Jean-François Méhaut visited M. Castro and L. Pilla at UFSC (October 2015) in the context of the Stic Amsud EnergySFE project.

9. Dissemination

9.1. Promoting Scientific Activities

9.1.1. Scientific events organisation

9.1.1.1. Member of the organizing committees

- Fabrice Rastello: Publication Chair ACM/IEEE CGO 2015
- Fabrice Rastello: Steering Committee Journées française de la compilation
- Fabrice Rastello: Steering Committee ACM/IEEE CGO

- Frédéric Desprez:Steering committee for the ISC Cloud & Big Data conference 2015
- Frédéric Desprez: General chair of VTDC 2015 (workshop within HPDC 2015)
- Ylies Falcone: Chair of the second international competition on Runtime Verification (CRV 15)

9.1.2. Scientific events selection

9.1.2.1. Chair of conference program committees

- Fabrice Rastello: Program Chair ACM/IEEE CGO 2016
- Frédéric Desprez: Program co-chair BigDataCloud'2015 (workshop within EuroPAR 2015)
- Frédéric Desprez: Global chair of topic "Grid, Cluster and Cloud Computing" within EuroPAR 2015

9.1.2.2. Member of the conference program committees

- Fabrice Rastello: ACM/IEEE CGO 2016
- Fabrice Rastello: CRI 2015
- Alain Ketterlin: ACM/IEEE CGO 2016
- Frédéric Desprez: ACM/IEEE CCGrid 2015
- Frédéric Desprez: CLOSER 2015
- Frédéric Desprez: Workshop Committee at the 2015 ACM/IEEE Supercomputing Conference 2015
- Frédéric Desprez: IEEE CAC 2015
- Frédéric Desprez: IEEE Cluster 2015
- Ylies Falcone SAC-SVT 2015
- Ylies Falcone IPAC 2015
- Ylies Falcone CRI 2015
- Ylies Falcone MSR 2015
- Ylies Falcone PCODA 2015

9.1.2.3. Reviewer

- François Broquedis: EUROPAR 2015, SAC 2015
- Brice Videau: EUROPAR 2015, SAC 2015, IPDPS 2015, COMPASS 2015
- Ylies Falcone MSR 2015, RV 2015, ASE 2015, OOPSLA 2015, FM 2015, CAV 2015, DAC2015, DATE 2015

9.1.3. Journal

9.1.3.1. Reviewer - Reviewing activities

- Fabrice Rastello: ACM TACO, ACM TOCS
- François Broquedis: ACM TACO
- Brice Videau: ACM TACO, PARCO, JPDC
- Kevin Pouget: ACM TACO
- Frédéric Desprez: JPDC
- Frédéric Desprez: Journal of Supercomputing
- Ylies Falcone Formal Methods in System Design, International Journal of Information and Computer Security, Science of Computer Programming, Software Tools for Technology Transfer, Journal of Systems and Software, ACM Transaction on Aspect-Oriented Development, The Computer Journal, ACM Transactions on Information and System Security, Elsevier Computer Review, Software Testing, Verification and Reliability.

9.1.4. Invited talks

- HiPEAC ACACES Summer School 2015 (teacher): "SSA-based Compiler Design"

- Fabrice Rastello: LLNL, Apple Dec 2015: “Toward Automatic Characterisation of the Data Access Complexity of Programs”
- Frédéric Desprez: Inria/EPFL Workshop, Jan. 2015: “Grid’5000: Running a Large Instrument for Parallel and Distributed Computing Experiments”
- Jean-François Méhaut, Maison de la simulation, Saclay, France, March 2015: “BOAST: Un environnement de metaprogrammationpour une génération de code portable et efficace des noyaux de calcul HPC”
- Jean-François Méhaut, Laboratoire Jacques-Louis Lions, Paris, France, Journées inagurales de la machine de calcul, June 2015: “BOAST: Programmation des noyaux de calcul pour les projets européens Mont-Blanc”
- Jean-François Méhaut, Federal University of Santa Catarina, Florianaolis, Brazil, October 2015: “CORSE: Compiler Optimizations and Rntime SystEms”

9.1.5. Scientific expertise

- Frédéric Desprez: Referee for the Research Council of Norway
- Frédéric Desprez: ANR
- Frédéric Desprez: Reviewer for a project within the FET Initiatives in FP7 of the European Commission
- Ylies Falcone Representative of France in the COST Action ARVI
- Ylies Falcone COST Action ARVI, co-leader of Working Group on Core Runtime Verification
- Jean-François Mehaut Eurolab-4-HPC EU action, member of the panel

9.1.6. Research administration

- Frédéric Desprez: Deputy Scientific Director at Inria
- Frédéric Desprez: Director of the GIS GRID5000

9.2. Teaching - Supervision - Juries

9.2.1. Teaching

Master : Fabrice Rastello (external intervention), Programming Languages and Compiler Design, 3 hours, M1 of international MoSIG, UJF, Grenoble, France

Master and PhD: Jean-François Méhaut, Parallel Programming, 40 hours, University of Yaoundé 1, LIRIMA, CETIC, February 2015

Master I: Jean-François Méhaut, Operating System Design, 50 hours, Polytech Grenoble

L3, Jean-François Méhaut, Numerical Methods, 50 hours, Polytech Grenoble,

M1, Jean-François Méhaut, Operating System Project, 20 hours, UFR IM2AG

L3, Jean-François Méhaut, Advanced Algorithm, 50 hours, UFR IM2AG

L3, François Broquedis, Introduction to algorithms and programming, 80 hours, Grenoble Institute of Technology (ENSIMAG)

L3, François Broquedis, Introduction to UNIX, 20 hours, Grenoble Institute of Technology (ENSIMAG)

L3, François Broquedis, C programming, 50 hours, Grenoble Institute of Technology (ENSIMAG)

M1, François Broquedis, Operating Systems and Parallel Programming, 20 hours, Grenoble Institute of Technology (ENSIMAG)

M1, François Broquedis, Operating Systems Project, 20 hours, Grenoble Institute of Technology (ENSIMAG)

M2, François Broquedis, Parallel and Distributed Programming, Grenoble Institute of Technology (ENSIMAG)

Master, Florent Bouchez Tichadou, Compilation project, 15.5 hours, M1 Info & M1 MoSig, UFR IM2AG

Licence, Florent Bouchez Tichadou, C programming, 33 hours, L3, Grenoble Institute of Technology (ENSIMAG)

Master, Florent Bouchez Tichadou, Algorithms and Program Design, 33 hours, M1 MoSIG, UFR IM2AG

Licence, Florent Bouchez Tichadou, Algorithms languages and programming, 71 hours, L2, UFR IM2AG

Master, Florent Bouchez Tichadou, Operating Systems, 28.5 hours, M1 Info, UFR IM2AG

Master, Ylies Falcone Programming Language Semantics and Compiler Design, MoSIG, 66 hours

License, Ylies Falcone Languages and Automata, UJF, 105 hours

Master, Ylies Falcone is co-responsible of the first year of the International Master of Computer Science (Univ. Grenoble Alpes and INP ENSIMAG)

9.2.2. Supervision

9.2.2.1. Fabrice Rastello

PhD in progress: Duco van Amstel, Scheduling and optimization for memory locality of dataflow programs on many-core processors, April 1st 2013, advised by Fabrice Rastello and Benoit Dupont-de-Dinechin

PhD in progress: Diogo Sampaio, Profiling Guided Hybrid Compilation, October 8 2013, advised by Fabrice Rastello

PhD in progress: François Gindraud, Semantics and compilation for a data-flow model with a global address space and software cache coherency, January 1st 2013, advised by Fabrice Rastello and Albert Cohen.

PhD in progress: Venmugil Elango, Dynamic Analysis for Characterization of Data Locality Potential, September 2010, advised by Fabrice Rastello and P. Sadayappan.

9.2.2.2. Jean-François Méhaut

PhD in progress: Serge Emteu, CIFRE ST Microelectronics, advised by Miguel Santan (STM), Alexandre Termier (Dream/Irisa), Jean-François Méhaut

PhD in progress: Oleg Iegorov, advised by Alexandre Termier (Dream/Irisa) and Jean-François Méhaut

PhD in progress: Nassim Halli, CIFRE with Asselta, advised by Henri-Pierre Charles (CEA/DRT List, CRI PILSI), Jean-François Méhaut

PhD in progress: Naweiluo Zhou, advised by Eric Rutten (Inria, CtrlA), Gwenael Delaval (UGA, CtrlA), Jean-François Méhaut

PhD in progress: Thomas Messi Nguelé, advised by Maurice Tchuenté (Yaoundé I, LIRIMA) and Jean-François Méhaut

PhD in progress: Thomas Goncalves, advised by Marc Perache (CEA/DAM), Frédéric Desprez, Jean-François Méhaut

PhD in progress: Vanessa Vargas, advised by Raoul Velzco (CNRS, TIMA) and Jean-François Méhaut

9.2.2.3. Frédéric Desprez

PhD in progress: Jonathan Pastor, advised by Frédéric Desprez, Adrien Lèbre (EMN Nantes, Ascola team)

PhD in progress: Pedro Silva, advised by Frédéric Desprez, C. Perez (Inria, Avalon team)

PhD in progress: Georgios Christodoulis, advised by Frederic Desprez, Olivier Muller (TIMA/SLS) and François Broquedis

PhD in progress: Thomas Goncalves, advised by Marc Perache (CEA/DAM), Frédéric Desprez, Jean-François Méhaut

9.2.2.4. François Broquedis

PhD in progress: Georgios Christodoulis, *Adaptation of a heterogeneous runtime system to efficiently exploit FPGA* advised by Frederic Desprez, Olivier Muller (TIMA/SLS) and François Broquedis

PhD in progress: Philippe Virouleau, *Improving the performance of task-based runtime systems on large scale NUMA machines*, co-advised by Thierry Gautier (Inria/AVALON), Raymond Namyst (Inria/STORM), Bruno Raffin (Inria/MOAIS), François Broquedis

Engineer internship: Olivier Soldano, *Efficient execution of OpenMP applications: a compiler/runtime cooperation*, co-advised by Jean-François Méhaut and François Broquedis

9.2.2.5. Ylies Falcone

PhD in progress: Antoine El-Hokayem, Decentralised and Distributed Monitoring of Cyber-Physical Systems

PhD defended: Abdurrahman Pektas, *Behavior based malware classification using online machine learning*, co-advised by Jean-Claude Fernandez (Vérimag)

9.2.3. Juries

9.2.3.1. Fabrice Rastello

Emmanuelle Saillard, Reviewer, *Static/Dynamic Analyses for Validation and Improvement of Multi-models HPC Applications*, PhD of the University of Bordeaux, 24/05/15

9.2.3.2. Jean-François Méhaut

PhD: Ashraf Elantably, *Study of task migration in a multi-tiles architecture: Automatic generation of an agent based solution*, Université de Grenoble, TIMA, 16/12/2015

PhD: Pei Li, *Système Unifié de transformation de code et d'exécution pour un passage aux architectures multi-coeurs hétérogènes*, Université de Bordeaux, Inria/Storm, Telecom SudParis, 17/12/2015

PhD: Anastasia Butko, *Fast Cycle-approximate Simulation Techniques for Manycore Architecture Exploration*, Université de Montpellier, LIRMM, 10/12/2015

PhD: Fabien Rozar, *Contributions à l'amélioration de l'extensibilité de simulations parallèles de plasmas turbulents*, Université de Bordeaux, CEA Cadarache, Maison de la simulation Saclay, 5/11/2015

PhD: Mohamed Bergach, *Adaptation de la Transformée de Fourier rapide sur une architecture mixte CPU/GPU intégrée*, Université de Nice Sophia Antipolis, 2/10/2015

PhD: Andi Drebes, *Dynamic Optimization of Data-flow task-parallel applications for large scale NUMA systems*, Université Pierre et Marie Curie, 25/6/2015

PhD: Corentin Rossignon, *Un modèle de programmation à grain fin pour la parallélisation de solveurs linéaires creux*, Université de Bordeaux, Inria/Storm, Total, 17/07/2015

PhD: Abal Cheick Ahamed, *Méthodes Numériques pour la résolution accélérée des systèmes linéaires de grandes tailles sur architectures hybrides massivement parallèles*, Ecole Centrale de Paris, 7/7/2015

HDR: Patrick Carribault, *Compiler/Runtime Cooperation for Multi-Paradigm Parallelism*, Université de Versailles Saint Quentin en Yveline, CEA Bruyères, 8/7/2015

HDR: Marc Perache, *Vers des supports exécutifs et des outils de profilage adaptés aux architectures many/multi coeurs dans le cadre du calcul hautes performances*, Université de Versailles Saint-Quentin en Yvelines, CEA Bruyères, 3/11/2015

9.2.3.3. Frédéric Desprez

PhD: Xavier Lacoste, Reviewer, *Scheduling and memory optimizations for sparse direct solver on multi-core/multi-gpu cluster systems*, Université de Bordeaux, 18/02/15

PhD: Sylvain Gault, *Improving MapReduce Performance on Clusters*, Ecole normale supérieure de Lyon, 23/03/15

HDR: Philippe Merle, Reviewer, *Intergiciel d'intergiciels adaptable à base de Services, Composants et Aspects* , Université de Lille3, 24/09/15

PhD: Emmanuel Cieren, Reviewer, *Molecular Dynamics for Exascale Supercomputers*, Université de Bordeaux, 09/10/15

PhD: Astrid Casadei, *Optimisations des solveurs linéaires creux hybrides basés sur une approche par complément de Schur et décomposition de domaine*, Université de Bordeaux, 19/10/15

HDR: Sébastien Monnet, *Contributions à la réplication de données dans les systèmes distribués à grande échelle*, Université Pierre et Marie Curie, 03/11/15

HDR: Georges Da Costa, *Évaluation et optimisation de performance énergétique des centres de calcul*, Université de Toulouse 3 Paul Sabatier, 12/11/15

HDR: Patricia Stolf, Reviewer, *La gestion des ressources pour des infrastructures vertes par la reconfiguration*, Université de Toulouse 3 Paul Sabatier, 13/12/15

PhD: Florent Lopez, *Solveur multifrontal QR à base de tâches pour architectures hétérogènes*, Université de Toulouse 3 Paul Sabatier, 11/12/15

9.2.3.4. Ylies Falcone

PhD: reviewer of the thesis of Eric Lupaud Ngoupé (University of Québec at Chicoutimi).

PhD: examiner of the thesis of Srinivas Pinisetty (Inria Rennes) on *Runtime Enforcement of Timed Properties*

10. Bibliography

Publications of the year

Doctoral Dissertations and Habilitation Theses

[1] S. V. EMTEU TCHAGOU. *Reducing trace size in multimedia applications endurance tests*, Université de Grenoble Alpes, December 2015, https://hal.archives-ouvertes.fr/tel-01251336

[2] L. STANISIC. *A Reproducible Research Methodology for Designing and Conducting Faithful Simulations of Dynamic Task-based Scientific Applications*, Université Grenoble Alpes, October 2015, https://tel.archives-ouvertes.fr/tel-01248109

Articles in International Peer-Reviewed Journals

[3] V. ELANGO, N. SEDAGHATI, F. RASTELLO, L.-N. POUCHET, J. RAMANUJAM, R. TEODORESCU, P. SADAYAPPAN. *On Using the Roofline Model with Lower Bounds on Data Movement*, in "ACM Transactions on Architecture and Code Optimization (TACO) ", January 2015, vol. 11, n^{o} 4, pp. 67:1–67:23, https://hal.inria.fr/hal-01104765

[4] Y. FALCONE, M. JABER, T.-H. NGUYEN, M. BOZGA, S. BENSALEM. *Runtime verification of component-based systems in the BIP framework with formally-proved sound and complete instrumentation*, in "Software and Systems Modeling", 2015, vol. 14, n° 1, 38 p. [*DOI :* 10.1007/s10270-013-0323-y], https://hal.inria.fr/hal-01248420

[5] Y. FALCONE, L. D. ZUCK. *Runtime Verification: the Application Perspective*, in "International Journal on Software Tools for Technology Transfer", April 2015, vol. 17, n° 2, 3 p. [*DOI :* 10.1007/s10009-014-0360-z], https://hal.inria.fr/hal-01248423

[6] E. FRANCESQUINI, M. CASTRO, P. H. PENNA, F. DUPROS, H. C. D. FREITAS, P. O. A. NAVAUX, J.-F. MÉHAUT. *On the Energy Efficiency and Performance of Irregular Application Executions on Multicore, NUMA and Manycore Platforms*, in "Journal of Parallel and Distributed Computing", February 2015, vol. 76, pp. 32-48 [*DOI :* 10.1016/j.jpdc.2014.11.002], https://hal-brgm.archives-ouvertes.fr/hal-01092325

[7] E. L. PADOIN, F. Z. BOITO, L. L. PILLA, M. BASTOS CASTRO, P. O. A. NAVAUX, J.-F. MEHAUT. *Performance/energy trade-off in scientific computing: the case of ARM big.LITTLE and Intel Sandy Bridge*, in "IET Computers and Digital Techniques", January 2015, vol. 9, n° 1, pp. 1-9 [*DOI :* 10.1049/iet-cdt.2014.0074], https://hal.archives-ouvertes.fr/hal-01127697

[8] L. PILLA, T. BOZETTI, M. CASTRO, P. O. A. NAVAUX, J.-F. MÉHAUT. *ComprehensiveBench: a Benchmark for the Extensive Evaluation of Global Scheduling Algorithms*, in "Journal of Physics: Conference Series", September 2015, pp. 1-12, https://hal.archives-ouvertes.fr/hal-01183558

[9] L. STANISIC, S. THIBAULT, A. LEGRAND, B. VIDEAU, J.-F. MÉHAUT. *Faithful Performance Prediction of a Dynamic Task-Based Runtime System for Heterogeneous Multi-Core Architectures*, in "Concurrency and Computation: Practice and Experience", May 2015, 16 p. [*DOI :* 10.1002/cpe], https://hal.inria.fr/hal-01147997

International Conferences with Proceedings

[10] W. BAO, K. SRIRAM, L.-N. POUCHET, F. RASTELLO, P. SADAYAPPAN. *PolyCheck: Dynamic Verification of Iteration Space Transformations on Affine Programs*, in "Proceedings of the 43nd Annual ACM SIGPLAN-SIGACT Symposium on Principles of Programming Languages, POPL 2016", St Petersburg, United States, ACM, January 2016, https://hal.inria.fr/hal-01234104

[11] P. DAIAN, Y. FALCONE, P. MEREDITH, T. F. SERBANUTA, S. SHIRIASHI, A. IWAI, G. ROSU. *RV-Android: Efficient Parametric Android Runtime Verification, a Brief Tutorial*, in "6th International Conference, RV 2015, September 22-25, Proceedings", Vienne, Austria, Runtime Verification, Springer, September 2015, vol. LNCS, n° 9333, 16 p. [*DOI :* 10.1007/978-3-319-23820-3_24], https://hal.inria.fr/hal-01248350

[12] V. ELANGO, F. RASTELLO, L.-N. POUCHET, J. RAMANUJAM, P. SADAYAPPAN. *On Characterizing the Data Access Complexity of Programs*, in "42nd Annual ACM SIGPLAN-SIGACT Symposium on Principles of Programming Languages, POPL 2015", Mumbai, India, ACM, January 2015, pp. 567-580, https://hal.inria.fr/hal-01104556

[13] S. V. EMTEU TCHAGOU, A. TERMIER, J.-F. MÉHAUT, B. VIDEAU, M. SANTANA, R. QUINIOU. *Reducing trace size in multimedia applications endurance tests*, in "Design, Automation & Test in Europe Conference & Exhibition (DATE)", Grenoble, France, 2015, https://hal.archives-ouvertes.fr/hal-01093576

[14] O. IEGOROV, A. TERMIER, V. LEROY, J.-F. MÉHAUT, M. SANTANA. *Data Mining Approach to Temporal Debugging of Embedded Streaming Applications*, in "15th International Conference on Embedded Software (EMSOFT'2015)", Amsterdam, Netherlands, October 2015, https://hal.archives-ouvertes.fr/hal-01178782

[15] A. KASSEM, Y. FALCONE, P. LAFOURCADE. *Monitoring Electronic Exams*, in "6th International Conference, RV 2015, September 22-25, Proceedings", Vienne, Australia, Runtime Verification, Springer, September 2015, vol. 9333, 16 p. [*DOI :* 10.1007/978-3-319-23820-3_8], https://hal.inria.fr/hal-01248349

[16] S. PINISETTY, Y. FALCONE, T. JÉRON, H. MARCHAND. *TiPEX: A Tool Chain for Timed Property Enforcement During eXecution*, in "RV'2015, 6th International Conference on Runtime Verification", Vienne, Austria, E. BARTOCCI, R. MAJUMDAR (editors), Lecture Notes in Computer Science, Springer, September 2015, vol. 9333, 12 p. [*DOI :* 10.1007/978-3-319-23820-3_22], https://hal.inria.fr/hal-01244446

[17] M. RENARD, Y. FALCONE, A. ROLLET, S. PINISETTY, T. JÉRON, H. MARCHAND. *Enforcement of (Timed) Properties with Uncontrollable Events*, in "12th International Colloquium on Theoretical Aspects of Computing (ICTAC 2015)", Cali, Colombia, Theoretical Aspects of Computing - ICTAC 2015, Springer, October 2015, vol. LNCS, n^{o} 9399, 22 p. [*DOI :* 10.1007/978-3-319-25150-9_31], https://hal.inria.fr/hal-01185238

[18] L. STANISIC, E. AGULLO, A. BUTTARI, A. GUERMOUCHE, A. LEGRAND, F. LOPEZ, B. VIDEAU. *Fast and Accurate Simulation of Multithreaded Sparse Linear Algebra Solvers*, in "The 21st IEEE International Conference on Parallel and Distributed Systems", Melbourne, Australia, The 21st IEEE International Conference on Parallel and Distributed Systems, December 2015, https://hal.inria.fr/hal-01180272

[19] F. GRUBER, J. DOERFERT, A. LAMBRINEAS, T. GROSSER, F. RASTELLO, F. MAGNO QUINTÃO PEREIRA. *Runtime pointer disambiguation*, in "Proceedings of the 2015 ACM SIGPLAN International Conference on Object-Oriented Programming, Systems, Languages, and Applications, OOPSLA 2015", Pittsburgh, United States, ACM, October 2015, 18 p. , https://hal.inria.fr/hal-01234086

Conferences without Proceedings

[20] H. CHARAFEDDINE, K. EL-HARAKE, Y. FALCONE, M. JABER. *Runtime Enforcement for Component-Based Systems*, in "Symposium on Applied Computing - Software Verification and Testing", Salamanque, Spain, April 2015 [*DOI :* 10.1145/2695664.2695879], https://hal.inria.fr/hal-01248353

[21] Y. FALCONE, D. NICKOVIC, G. REGER, D. THOMA. *Second International Competition on Runtime Verification*, in "6th International Conference, RV 2015, September 22-25, Proceedings", Vienne, Austria, Springer, September 2015, vol. LNCS, n^{o} 9333, 16 p. [*DOI :* 10.1007/978-3-319-23820-3_27], https://hal.inria.fr/hal-01248351

[22] N. A. HALLI, H.-P. CHARLES, J.-F. MEHAUT. *Performance comparison between Java and JNI for optimal implementation of computational micro-kernels*, in "5th International Workshop on Adaptive Self-tuning Computing Systems (ADAPT'15)", Amsterdam, Netherlands, January 2015, Part of ADAPT Workshop proceedings, 2015 (arXiv:1412.2347), https://hal.archives-ouvertes.fr/hal-01127712

[23] T. MESSI NGUÉLÉ, M. TCHUENTÉ, J.-F. MEHAUT. *Exploitation de la structure en communautés pour la réduction de défauts de cache dans la fouille des réseaux sociaux*, in "Conférence de Recherche en Informatique (CRI)", Yaoundé, Cameroon, December 2015, https://hal.archives-ouvertes.fr/hal-01252798

[24] P. H. PENNA, M. CASTRO, H. FREITAS, F. BROQUEDIS, J.-F. MÉHAUT. *Uma Metodologia Baseada em Simulação e Algoritmo Genético para Exploração de Estratégias de Escalonamento de Laços*, in "Simpósio em Sistemas Computacionais de Alto Desempenho (WSCAD)", Florianópolis, Brazil, SBC, October 2015, https://hal.archives-ouvertes.fr/hal-01239916

[25] S. SAIDI, Y. FALCONE. *Dynamic Detection and Mitigation of DMA Races in MPSoCs*, in "18th Euromicro Conference on Digital Systems Design (DSD 2015)", Madeire, Portugal, August 2015 [*DOI :* 10.1109/DSD.2015.77], https://hal.inria.fr/hal-01248352

Scientific Books (or Scientific Book chapters)

[26] L. GENOVESE, B. VIDEAU, D. CALISTE, J.-F. MÉHAUT, S. GOEDECKER, T. DEUTSCH. *Wavelet-Based Density Functional Theory on Massively Parallel Hybrid Architectures*, in "Electronic Structure Calculations on Graphics Processing Units: From Quantum Chemistry to Condensed Matter Physics", R. WALKER (editor), Wiley-Blackwell, February 2016, https://hal.archives-ouvertes.fr/hal-01239245

Scientific Popularization

[27] F. BODIN, J.-F. MÉHAUT. *Programmation et Exploitation des Platesformes HPC:Défis et challenges*, in "Clés du futur", TERATEC, June 2015, https://hal.archives-ouvertes.fr/hal-01174302