IN PARTNERSHIP WITH:
Institut polytechnique de Grenoble

Université de Grenoble Alpes

Activity Report 2017

Project-Team CORSE

Compiler Optimization and Run-time SystEms

IN COLLABORATION WITH: Laboratoire d'Informatique de Grenoble (LIG)

RESEARCH CENTER
Grenoble - Rhône-Alpes

THEME
Architecture, Languages and Compilation

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Creation of the Team: 2014 November 01, updated into Project-Team: 2016 July 01

CORSE *is located at Giant/Minatec in Grenoble.*

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1. Personnel

Research Scientists

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Post-Doctoral Fellows

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Administrative Assistants

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Latifa Boudiba [LIG]

Visiting Scientist

Julien Langou [University of Colorado Denver, until Jun 2017]

External Collaborator

Brice Videau [CEA, from Mar 2017]

2. Overall Objectives

2.1. Overall Objectives

Languages, compilers, and run-time systems are some of the most important components to bridge the gap between applications and hardware. With the continuous increasing power of computers, expectations are evolving, with more and more ambitious, *computational intensive and complex applications*. As desktop PCs are becoming a niche and servers mainstream, three categories of computing impose themselves for the next decade: mobile, cloud, and super-computing. Thus *diversity, heterogeneity* (even on a single chip) and thus also *hardware virtualization* is putting more and more pressure both on compilers and run-time systems. However, because of the energy wall, *architectures* are becoming more and more *complex* and *parallelism ubiquitous* at every level. Unfortunately, the memory-CPU gap continues to increase and energy consumption remains an important issue for future platforms. To address the challenge of *performance and energy consumption* raised by silicon companies, compilers and run-time systems must *evolve* and, in particular, interact, *taking into account the complexity of the target architecture*.

The overall objective of CORSE is to address this challenge by *combining static and dynamic compilation* techniques, with more interactive *embedding of programs and compiler environment in the run-time system*.

3. Research Program

3.1. Scientific Foundations

One of the characteristics of CORSE is to base our researches on diverse advanced mathematical tools. Compiler optimization requires the usage of the several tools around discrete mathematics: combinatorial optimization, algorithmic, and graph theory. The aim of CORSE is to tackle optimization not only for regular but also for irregular applications. We believe that new challenges in compiler technology design and in particular for split compilation should also take advantage of graph labeling techniques. In addition to run-time and compiler techniques for program instrumentation, hybrid analysis and compilation advances will be mainly based on polynomial and linear algebra.

The other specificity of CORSE is to address technical challenges related to compiler technology, run-time systems, and hardware characteristics. This implies mastering the details of each. This is especially important as any optimization is based on a reasonably accurate model. Compiler expertise will be used in modeling applications (e.g. through automatic analysis of memory and computational complexity); Run-time expertise will be used in modeling the concurrent activities and overhead due to contention (including memory management); Hardware expertise will be extensively used in modeling physical resources and hardware mechanisms (including synchronization, pipelines, etc.).

The core foundation of the team is related to the combination of static and dynamic techniques, of compilation, and run-time systems. We believe this to be essential in addressing high-performance and low energy challenges in the context of new important changes shown by current application, software, and architecture trends.

Our project is structured along two main directions. The first direction belongs to the area of run-time systems with the objective of developing strong relations with compilers. The second direction belongs to the area of compiler analysis and optimization with the objective of combining dynamic analysis and optimization with static techniques. The aim of CORSE is to ground those two research activities on the development of the end-to-end optimization of some specific domain applications.

4. Application Domains

4.1. Transfer

The main industrial sector related to the research activities of CORSE is the one of semi-conductor (programmable architectures spanning from embedded systems to servers). Obviously any computing application which has the objective of exploiting as much as possible the resources (in terms of high-performance but also low energy consumption) of the host architecture is intended to take advantage of advances in compiler and run-time technology. These applications are based over numerical kernels (linear algebra, FFT, convolution...) that can be adapted on a large spectrum of architectures. Members of CORSE already maintain fruitful and strong collaborations with several companies such as STMicroelectronics, Bull, UpMem, Kalray, or Aselta.

5. New Software and Platforms

5.1. THEMIS

THEMIS: A Tool for Decentralized Monitoring Algorithms
KEYWORDS: Monitoring - Simulation
FUNCTIONAL DESCRIPTION: THEMIS consists of a library and command-line tools. It provides an API, data structures and measures for decentralized monitoring. These building blocks can be reused or extended to modify existing algorithms, design new more intricate algorithms, and elaborate new approaches to assess existing algorithms.

- Participants: Antoine El Hokayem and Ylies Falcone
- Contact: Antoine El Hokayem
- Publications: THEMIS: A Tool for Decentralized Monitoring Algorithms - Monitoring Decentralized Specifications
- URL: https://gitlab.inria.fr/monitoring/themis/

5.2. Verde

KEYWORDS: Debug - Verification
FUNCTIONAL DESCRIPTION: Interactive Debugging with a traditional debugger can be tedious. One has to manually run a program step by step and set breakpoints to track a bug.

i-RV is an approach to bug fixing that aims to help developpers during their Interactive Debbugging sessions using Runtime Verification.

Verde is the reference implementation of i-RV.

- Participants: Kevin Pouget, Ylies Falcone, Raphael Jakse and Jean-François Méhaut
- Contact: Raphael Jakse
- Publication: Interactive Runtime Verification - When Interactive Debugging meets Runtime Verification
- URL: https://gitlab.inria.fr/monitoring/verde

5.3. Nanvix

KEYWORD: Operating system

SCIENTIFIC DESCRIPTION: Nanvix presents a similar structure to Unix System V , and it has been intentionally designed this way because it is adopted in some successful Operating Systemes, such as Linux. Nanvix is structured in two layers. The kernel (bottom layer), seats on top of the hardware and runs in privileged mode. Its job is to (i) extend the underlying hardware so that an easier-to-program interface is exported to the higher layer, and (ii) multiplex hardware resources among several users. The userland (top layer), relies on Posix system calls exported by the kernel and it is the place where user software run in unprivileged mode.

The kernel presents a tiny monolithic architecture (7k loc), and it is structured in four subsystems: the hardware abstraction layer, the memory management system, the process manager, and the file system. The hardware abstraction layer interacts directly with the hardware and exports to the other subsystems a set of well-defined low-level routines. The job of the hardware abstraction layer is to isolate, as much as possible, all the hardware intricacies, so that the kernel can easily be ported to other compatible platforms.

The memory manager provides a flat virtual memory abstraction. It does so by having two modules working together: the paging and virtual memory allocator. The former deals with paging, keeping in memory those pages that are more frequently used, and swapping out to disk those that are not. The virtual memory allocator, on the other hand, relies on the paging module to create higher-level abstractions called memory regions, and thus enable advanced features such as shared memory regions, on-demand loading and lazy coping.

The process manager handles creation, termination, scheduling, synchronization and communication of processes. Processes are single-threaded entities and are created on demand, either by the system itself or the user. Scheduling is based on preemption, and in userland it happens whenever a process runs out of quantum or blocks awaiting for a resource. In kernel land, processes run in nonpreemptive mode and scheduling occurs when a processes voluntarily foes to sleep. In addition, the process manager exports inter-process communication facilities, such as Posix pipes and shared memory regions.

The file system provides a uniform interface for dealing with hardware resources. It extends the device driver interface and creates on top of it the file abstraction. Files can be accessed through a unique pathname, and may be shared among several processes. The Nanvix file system is compatible with the one present in Minix, it adopts an hierarchical inode structure, and features mounting points and disk block caching.

Investigations on Nanvix concern to a joint collaboration research effort between the CORSE Team (Inria - FRANCE) and CArT (PUC Minas - Brazil). More precisely, a port of Nanvix to low-power embedded many-cores is ongoing, and it consists on the thesis subject of a cotutella student between the two aforementioned research teams.
FUNCTIONAL DESCRIPTION: Nanvix is an Operating System that we designed from scratch to address growing interested on research and education. It originally targets x86-based architectures and features virtual-memory based on paging, a hierarchical Unix file system based on inodes, a uniform device driver interface, and a preemptive priority-based scheduler.

We are currently extending Nanvix to provide a portable OS targetting multiple manycore platforms through the PhD of Pedro Henrique Penna.

- Participants: Pedro Henrique De Mello Morado Penna, François Broquedis, Jean-François Méhaut, Marcio Bastos Castro and Henrique Cota De Freitas
- Partner: Université pontificale catholique du Minas Gerais
- Contact: Pedro Henrique De Mello Morado Penna
- URL: https://github.com/nanvix/nanvix

5.4. Mickey

KEYWORDS: Dynamic Analysis - Performance analysis - Profiling - Polyhedral compilation
FUNCTIONAL DESCRIPTION: Mickey is a set of tools for profiling based performance debugging for compiled binaries. It uses a dynamic binary translator to instrument arbitrary programs as they are being run to reconstruct the control flow and track data dependencies. This information is then fed to a polyhedral optimizer that proposes structured transformations for the original code.

Mickey can handle both inter- and intra-procedural control and data flow in a unified way, thus enabling inter-procedural structured transformations. It is based on QEMU to allow for portability, both in terms of targeted CPU architectures, but also in terms of programming environment and the use of third-party libraries for which no source code is available.

- Partner: STMicroelectronics
- Contact: Fabian Gruber

5.5. IPFME

Integer Polynomial Fourier-Motzkin Elimination
KEYWORDS: Fourier–Motzkin Elimination - Quantifier Elimination - System of Inequalities - Mixed Integer Programming - Polynomial or analytical systems
SCIENTIFIC DESCRIPTION: Fourier-Motzkin is a very well known algorithm for performing quantifier (variable) elimination, given a system (or formula) of inequalities. It removes quantified variables by combining all upper and lower bounds of such variables.

It was designed to operate on linear systems, where all coefficients of the variable being eliminated are numeric values, and the inequality can be classified as either a upper or lower bound.

When dealing with polynomials, variable coefficients might be symbolic expressions. In such case, all possible signs of the coefficient (positive, negative, or zero) must be explored.

To avoid this branching we use the positiveness test algorithm, proposed by Markus Schweighofer (https://doi.org/10.1016/S0022-4049(01)00041-X), to retrieve symbolic coefficient signs.

The same positiveness test algorithm is of major importance when resolving system over integer variables, instead of reals. It is used in many other techniques required to preserve the precision of the simplified formula, such as extending the normalization technique (https://doi.org/10.1145/125826.125848) to symbolic expressions, performing convex hull detection and removing redundant constraints. Such tester is implemented using GLPK (https://www.gnu.org/software/glpk).
FUNCTIONAL DESCRIPTION: Quantifier elimination is the process of removing existential variables of a given formula, obtaining one with less variables and that implies the original formula. This can also be viewed as a projection of the set of points (integer here) that satisfy the original formula onto a sub-vectorial space made up of all the non-eliminated variables. The obtained projection is an over-approximation of the exact projection. The goal of the process is to make it as tight as possible.

IPFME presents extensions to the Fourier-Motzkin quantifier elimination process. The developed techniques allow to derive more precise simplification operations when handling integer valued multivariate polynomial systems.

The implementation, in C++, uses GiNaC (https://www.ginac.de/) for the manipulation of symbolic expressions.

- Authors: Diogo Nunes Sampaio, Fabrice Rastello and Alain Ketterlin
- Contact: Diogo Nunes Sampaio
- Publications: Profile Guided Hybrid Compilation - Simplification and Run-time Resolution of Data Dependence Constraints for Loop Transformations

5.6. mcGDB

Model Centric Debugging with GDB
KEYWORDS: Model debugging - Parallel programming - OpenMP - Multicore

FUNCTIONAL DESCRIPTION: mcGDB defines the concept of "programming-model centric" source-level interactive debugging as an extension of the traditional language-level interactive debugging. The idea is to integrate into debuggers the notion of "programming models", as abstract machines running over the physical ones. These abstract machines, implemented by runtime libraries and programming frameworks, provide high-level primitives required for the implementation of today's parallel applications. mcGDB is developed as a Python extension of GDB, the debugger of the GNU project

- Partner: STMicroelectronics
- Contact: Jean-François Méhaut
- URL: http://dema.gforge.inria.fr/

5.7. BOAST

Bringing Optimization Through Automatic Source-to-Source Transformations
KEYWORDS: Code generation - Portability - Autotuning - High performance computing - Conformance testing - Productivity
FUNCTIONAL DESCRIPTION: BOAST provides scientific application developers with a framework to develop and test application computing kernels.

The developer starts from an application kernel (either designed or implemented), and writes it in a dedicated language. This language provides enough flexibility for the kernel to be metaprogrammed with several orthogonal optimizations. From this set of optimizations, possible languages targets, and compilation options, the user can design an optimization space to explore. This optimization space can contain rules to remove infeasible candidates. BOAST provides the mechanisms to specify those optimization spaces and enforce the users rules.

BOAST was already used with three real scientific applications: BigDFT (materials, CEA Inac), SPECFEM3D (geophysics, CNRS and Princeton) and GYSELA (plasma physics, CEA Cadarache, ITER). '

- Partner: CEA INAC LSim
- Contact: Brice Videau
- URL: https://github.com/Nanosim-LIG/boast

6. New Results

6.1. Simplification and Run-time Resolution of Data Dependence Constraints for Loop Transformations

Participants: Diogo Nunes Sampaio, Alain Ketterlin [Inria CAMUS], Louis-Noël Pouchet [CSU, USA], Fabrice Rastello.

Loop optimizations such as tiling, thread-level parallelization or vectorization are essential transformations to improve performance. Their use rely on the ability to compute dependence information at compile-time to assess their validity, but in many real situations, dependence analysis fails to provide precise enough information. Typical examples where this happens are when working over compilers IR (e.g., LLVM IR) or with legacy source code, with pointers and linearized arrays (e.g., packed symmetric matrices in BLAS LAPACK). In this scenario, the compiler will often be unable to apply aggressive transformations due to lack of conclusive static dependence analysis.

This work makes a fundamental leap towards enabling complex loop transformations in real-life scenarios, by using a hybrid static+dynamic analysis to disambiguate may-dependencies. Similarly to GCC's auto-vectorization, our approach consists in adding a lightweight run-time test to check whether ambiguous may-dependencies do exist at execution time, to determine whether the optimized or unmodified code version should be called. The main contribution of our work is to generalize this pragmatic approach to a large class of loop-nest transformations, including tiling, loop invariant code motion, parallelization, etc. In particular, we design a quantifier elimination scheme on integer multivariate-polynomials, which can aid application of off-the-shelf polyhedral transformations on a larger class of programs, that holds polynomial memory access and affine loop bounds.

The preciseness of the presented scheme and the low run-time overhead of the test are key to make this approach realistic. We experimentally validate our technique on 25 benchmarks using complex loop transformations, achieving negligible overhead. Preciseness is assessed by the observed success of generated test in practical cases.

IPFME tool 5.5 has been developped in this context. This work is the fruit of the collaboration 8.4.1.1 with OSU. It has been presented at the ACM/SIGARCH International Conference on Supercomputing, ICS 2017 [25].

6.2. Optimizing the Four-Index Integral Transform Using Data Movement Lower Bounds Analysis

Participants: Samyam Rajbhandari [Microsoft, USA], Fabrice Rastello, Karol Kowalski [PNNL, USA], Sriram Krishnamoorthy [PNNL, USA], P. Sadayappan [OSU, USA].

The four-index integral transform is a fundamental and computationally demanding calculation used in many computational chemistry suites such as NWChem. It transforms a four-dimensional tensor from an atomic basis to a molecular basis. This transformation is most efficiently implemented as a sequence of four tensor contractions that each contract a four-dimensional tensor with a two-dimensional transformation matrix. Differing degrees of permutation symmetry in the intermediate and final tensors in the sequence of contractions cause intermediate tensors to be much larger than the final tensor and limit the number of electronic states in the modeled systems.

Loop fusion, in conjunction with tiling, can be very effective in reducing the total space requirement, as well as data movement. However, the large number of possible choices for loop fusion and tiling, and data/computation distribution across a parallel system, make it challenging to develop an optimized parallel implementation for the four-index integral transform. We develop a novel approach to address this problem, using lower bounds modeling of data movement complexity. We establish relationships between available aggregate physical memory in a parallel computer system and ineffective fusion configurations, enabling their pruning and consequent identification of effective choices and a characterization of optimality criteria. This work has resulted in the development of a significantly improved implementation of the four-index transform that enables higher performance and the ability to model larger electronic systems than the current implementation in the NWChem quantum chemistry software suite.

This work is the fruit of the collaboration 8.4.1.1 with OSU. It has been presented at the ACM/SIGPLAN Symposium on Principles and Practice of Parallel Programming, PPoPP 2017 [21].

6.3. Register Optimizations for Stencils on GPUs

Participants: Aravind Sukumaran-Rajam [OSU, USA], Atanas Rountev [OSU, USA], Fabrice Rastello, Louis-Noël Pouchet [CSU, USA], P. Sadayappan [OSU, USA].

The recent advent of compute-intensive GPU architecture has allowed application developers to explore high-order 3D stencils for better computational accuracy. A common optimization strategy for such stencils is to expose sufficient data reuse by means such as loop unrolling, with the hope of register-level reuse. However, the resulting code is often highly constrained by register pressure. While the current state-of-the-art register allocators are satisfactory for most applications, they are unable to effectively manage register pressure for such complex high-order stencils, resulting in a sub-optimal code with a large number of register spills. In this paper, we develop a statement reordering framework that models stencil computations as DAG of trees with shared leaves, and adapts an optimal scheduling algorithm for minimizing register usage for expression trees. The effectiveness of the approach is demonstrated through experimental results on a range of stencils extracted from application codes.

This work is the fruit of the collaboration 8.4.1.1 with OSU. It will be presented at the ACM/SIGPLAN Symposium on Principles and Practice of Parallel Programming, PPoPP 2018.

6.4. Data-Flow/Dependence Profiling for Structured Transformations

Participants: Diogo Nunes Sampaio, Fabian Gruber, Christophe Guillon [STMicroelectronics], Antoine Moynault [STMicroelectronics], Louis-Noël Pouchet [CSU, USA], Fabrice Rastello.

Profiling feedback is an important technique used by developers for performance debugging, where it is usually used to pinpoint performance bottlenecks and also to find optimization opportunities. Assessing the validity and potential benefit of a program transformation requires accurate knowledge of the data flow and data dependencies, which can be uncovered by profiling a particular execution of the program.

In this work we develop MICKEY 5.4, an end-to-end infrastructure for dynamic binary analysis, which produces feedback about the potential to apply structured transformations to uncover non-trivial parallelism and data locality via complex program re-scheduling. Our tool can handle both inter- and intra-procedural aspects of the program in a unified way, thus enabling inter-procedural structured transformations. It is based on QEMU and uses dynamic binary translation to instrument arbitrary programs at run-time. The design of this tool was driven by the goal of achieving portability, both in terms of targeted CPU architectures, but also in terms of programming environment and the use of third-party libraries for which no source code is available.

This work is the fruit of the collaboration 8.4.1.1 with CSU and the contract 7.2 with STMicroelectronics.

6.5. Dynamic Load Balancing of Monte Carlo Particle Transport Applications

Participants: Thomas Gonçalves, Marc Pérache [CEA DAM, Bruyères le Châtel], Frederic Desprez, Jean-Francois Mehaut.

Monte Carlo particle transport applications consist in studying the behavior of particles moving about a simulation domain. Particle distribution among simulation domains is not uniform and changes dynamically during simulation. The parallelization of this kind of applications on massively parallel architectures leads to solve complex issues of workloads and data balancing among numerous compute cores.

This research work started by identifying parallelization pitfalls of Monte Carlo particle transport applications using theoretical and experimental analysis of reference parallelization methods. A semi-dynamic load-balancing based on partitioning techniques has then been proposed. Finally, we designed a dynamic approach which is able to redistribute workloads and data while keeping a low communication volume. Compared to the perfectly balanced domain replication method using strong scaling measurement, the dynamic approach leads both to speedups and reduction of memory footprint.

This work is part of the Thomas Gonçalves's PhD thesis defended in September 2017 at TERATEC (Bruyères le Châtel). The main contributions of this work were also presented in the ParCo conference [14] .

6.6. BOAST: A Meta-Programming Framework to Produce Portable and Efficient Computing Kernels for HPC Applications

Participants: Brice Videau, Kevin Pouget, Luigi Genovese [CEA Inac, Grenoble], Thierry Deutsch [CEA Inac, Grenoble], Dimitri Komatitsch [LMA, CNRS, Marseille], Frédéric Desprez, Jean-Francois Mehaut.

Application portability is an important issue that should be solved efficiently, especially given the large number of different processors now available for today's supercomputers. The work needed to get performance portability is a tedious task, even for experienced programmers. The availability of semi-automatic tools is therefore mandatory for the development of large simulation applications. Computing kernels' identification and optimization has to be carefully performed as they usually consume most of the computing resources.

BOAST is a framework (DSL and run-time) that aims at describing kernels in a high-level language and it allows the comparison of the performance of different versions of the code in a simple and seamless way. We described its application to three use cases from the Mont-Blanc project. Results are encouraging as BOAST proved to be a powerful and flexible tool that allowed gains in performance compared to hand-tuned codes. Performance portability of those codes is also improved.

This work was mainly developed by Brice Videau in the context of the Mont-Blanc FP7 European projects 8.3.1.1. It lead to a publication in the International Journal of High Performance Computing Applications (IJHPCA) [11] . A paper will also be published in 2018 describing the BOAST usage for the Gysela Application (see http://gyseladoc.gforge.inria.fr/).

6.7. Auto-tuning at Run-time with Multiple Implementations of OpenMP Tasks

Participants: Luis Felipe Garlet Millani, Lucas Mello Schnorr [UFRGS, Brazil], Jean-François Mehaut.

OpenMP established itself as the de facto standard for parallel programming in shared memory environments. It received many additions over the years enabling OpenMP to be used with heterogeneous systems. We propose an extension to the task pragma of OpenMP allowing it to provide multiple ways to compute the desired result. The run-time can thus be provided with implementations with different trade-offs.

With the use of the BOAST 5.7 auto-tuning framework, these implementations can be generated automatically before the execution. But within this framework, the auto-tuned kernel is selected in an environment different from that of an actual execution of the application. As a consequence, it may be the case that no interactions occur between different tasks during the auto-tuning, while, in the actual execution, tasks do affect each other due to shared resources like cache or memory bandwidth: Kernel selection done in isolation during the auto-tuning process is probably not the best choice for the embedded execution as part of the full application.

We propose dealing with this limitation by having the auto-tuning phase select not a single but a set of implementations, to be later further selected during execution. Our approach also permits the tuning of different parameters (such as memory accesses and number of operations), and allows to use whichever implementation is more adequate for the thread based on monitored load.

Our extension is implemented within the LLVM framework and Clang compiler front-end. Furthermore we extend the LLVM OpenMP Run-time to be aware of the multiple task implementations. We verify the efficacy of our proposal with the Ondes3D seismic wave simulator and a sparse matrix multiplication application.

6.8. Improving Characterization of NUMA Architectures through Applications' Kernels

Participants: Philippe Virouleau, Francois Broquedis, Thierry Gautier, Julien Langou [UCD, USA], Fabrice Rastello.

Programmers need tools to be able to study their applications. When targeting NUMA architectures, many existing tools allow to observe and identify the critical parts of the application. However there is a need for tools that enable programmers to clearly understand how critical parts of their applications behave, and how they could be improved on a given architecture.

In the context of data-flow applications each part - *task* - of the application is clearly identified in the data-flow graph. All manipulated data are also clearly available as, within such framework, they constitute what links tasks with one another.

On NUMA architectures, a task's execution time depends, among others, on both the core which executes the task and the NUMA node on which has been allocated its data. Assume one can characterize a task behavior (with regard to its execution context) as follow: run it in isolation from the overall application, and change various of its properties (such as the size of input or the placement of data). Then the scheduler of a run-time system can use this characteristic to improve the overall performance: It would have full information about what is running on the machine (e.g.: on the same NUMA node as the idle thread), and could sort the tasks ready for execution according to how good their behavior would be on the idle thread, given the current state.

We designed a tool which goal is to help the user execute a given *scenario* on the architecture. This scenario describes:

- What are the data and where to allocate them on the architecture
- What are the tasks to execute, where to execute them on the architecture, and with which data
- What are the characteristics to observe for each task (execution time, performance counters, ...)

The tool guarantees that the scenario will be executed correctly on the architecture, letting him focus on understanding on his application rather than taking care of the low level implementation details.

We applied this approach to a dense linear algebra algorithm: the Cholesky factorization. It has enabled us to profile the four kernels of the application by running them in various configurations of data placements, sizes, and concurrent workload. We believe we've tested enough configurations to reliably find the best and worst cases for all the kernels Assuming the behavior of the kernel stays the same within the application, we've been able to estimate upper-bound and lower-bound execution time for the overall application given those best and worst cases.

6.9. Workload-aware Loop Scheduling of Irregular Loops

Participants: Pedro Henrique de Mello Morado Penna, Marcio Castro [UFSC, Universidade Federal de Santa Catarina, Brazil], Henrique Cota de Freitas [Pontifical Catholic University of Minas Gerais, Brazil], Francois Broquedis, Jean-Francois Mehaut.

The input workload of an irregular application must be evenly distributed among its threads to enable cutting-edge performance. To address this need in OpenMP, several loop scheduling strategies were proposed. While having this ever-increasing number of strategies at disposal is helpful, it has become a non-trivial task to select the best one for a particular application. Nevertheless, this challenge becomes easier to be tackled when existing scheduling strategies are extensively evaluated. Therefore, we present a performance and scalability evaluation of the recently proposed loop scheduling strategy named Smart Round-Robin (SRR). To deliver a comprehensive analysis, we coupled a synthetic kernel benchmarking technique with several rigorous statistical tools, and considered OpenMP's Static and Dynamic loop schedulers as our baselines. Our results unveiled that SRR performs better on irregular applications with symmetric workloads and coarse-grained parallelization, achieving up to 1.9x and 1.5x speedup over OpenMP's Static and Dynamic schedulers, respectively.

This work laid the foundations of a collaboration between CORSE, the UFSC, and PUC Minas, that led to the publication of two conference papers (ICCS'17 [20], WSCAD'17 [27]) and one international journal paper (CCPE'17 [5]). The WSCAD'17 paper has also been selected to be extended for a special issue of the CCPE journal. This extension will be based on recent works with the MHM (Multiscale Hybrid-Mixed Methods) simulator developed at LNCC for the H2020 HPC4e project 8.3.1.3 between Europe and Brazil.

6.10. Error-Rate Prediction and Radiation Experiments on a 28nm Many-Core Processor

Participants: Vanessa Vargas [TIMA Labs Grenoble & ESPE, Ecuador], Pablo Ramos [TIMA Labs Grenoble & ESPE, Ecuador], Vincent Ray [kalray, Montbonnot Saint-Martin], Camille Jalier [kalray, Montbonnot Saint-Martin], Renaud Stevens [kalray, Montbonnot Saint-Martin], Benoît Dupont de Dinechin [kalray, Montbonnot Saint-Martin], Maud Baylac [LSPC Labs, Université Grenoble Alpes, CNRS/IN2P3], Francesca Villa [LSPC

Labs, Université Grenoble Alpes, CNRS/IN2P3], Solenne Rey [LSPC Labs, Université Grenoble Alpes, CNRS/IN2P3], Nacer-Eddine Zergainoh [TIMA Labs, Université Grenoble Alpes & CNRS], Jean-Francois Mehaut, Raoul Velazco [TIMA Labs, Université Grenoble Alpes & CNRS].

This work analyses the 14 MeV neutron sensitivity of the MPPA-256 many-core processor. Analysis results suggest that ECC and interleaving implemented in the shared memories of clusters are very effective to mitigate SEUs as all detected events of this type were corrected.

The evaluation of the device dynamic response shows that by enabling the cache memories, it is possible to gain in performance of the application without compromising reliability, as all the detected errors produced in data and instruction cache memories were corrected by the parity protection. The non-correctable errors that occurred in the different dynamic tests were produced by bit-flips in general purpose registers since registers do not implement any protection mechanism.

Results show that the predicted application error-rate is reasonably close to the measured one. Consequently, despite the complexity of the many-core processor, this work supports the relevance of the use of the CEU approach to predict the error-rate of applications implemented in such devices.

This work is part of the Vanessa Vargas's PhD thesis defended in April 2017. This PhD thesis was advised by Raoul Velazco (TIMA) and Jean-François Méhaut. Four of the authors worked for the Kalray company. The experiments under radiation were performed on the GENEPI2 platform of the LSPC laboratory. This work was also published in the IEEE Transactions on Nuclear Sciences [10]. It was partially funded by the STIC-Amsud EnergySFE project 8.4.2.

6.11. CAP Bench: A Benchmark Suite for Low-Power Many-Core Processors

Participants: Matheus Souza [PUC Minas], Pedro Henrique de Mello Morado Penna, Matheus Queiroz [PUC Minas], Alyson Pereira [UFSC], Luis Góes [PUC Minas], Henrique Cota de Freitas [PUC Minas], Márcio Castro [UFSC], Philippe Navaux [UFRGS], Jean-Francois Mehaut.

CAP Bench is an open source benchmark suite that includes parallel applications suitable to evaluate emerging low-power many-core processors such as MPPA-256. The benchmark contains a diverse set of applications that evaluated key aspects of MPPA-256, namely the use of its compute clusters, I/O subsystem, NoC and energy consumption. We expose development difficulties and potential bottlenecks that can stem from the shift in development paradigm when programming for low-power many-core architectures. The results showed us that different applications can have different performance bottlenecks, which is why a solid knowledge about the low-power many-core architecture is necessary for the development of efficient programs.

Our analysis shows that CAP Bench is prepared for the analysis of low-power many-core processors such as the MPPA-256, being scalable and concerned with new trends on this type of architectures. To achieve good performance and scalability, we developed applications considering aspects such as parallel patterns, load balance and architecture limitations. This allowed us to evaluate several aspects of the MPPA-256.

Our benchmark explores the hybrid programming model, which is a trend in low-power many- core processors, following parallel patterns. This enables us to verify that, in the case of MPPA-256, communication time may surpass computation time, which would ideally never occur. This behavior was highlighted by the LU application available in CAP Bench, which may indicate that the NoC should be improved to achieve better performance on NoC-bound applications. In this manner, CAP Bench comes up with the proposal to identify such bottlenecks, revealing potential improvements that might be done in future many-core architectures.

Application development challenges are still out there, and have to be solved to enable the evaluation of next generation many-core processors. As future work, we intend to incorporate other applications to the benchmark, to make it more diverse and allow for a better characterization of the architecture and its aspects. We also intend to extend the benchmark use to other many-core architectures, to achieve a broader understanding of them and the differences between many- core processors

This work was developed in the context of the EnergySFE STIC Amsud project 8.4.2. A description of CAP Bench has been published in the CCPE (Concurrency Computation: Practice and Experience) international journal [9] . CAP Bench will be used and extended during Pedro Henrique Penna's doctoral thesis.

6.12. Social Network Analysis on Multi-Core Architectures

Participants: Thomas Messi Nguele, Maurice Tchuente [Univ Yaoundé 1, LIRIMA], Jean-Francois Mehaut.

One of social graph properties is the community structure, that is, subsets where nodes belonging to the same subset have a higher link density between themselves and a low link density with nodes belonging to external subsets. Furthermore, most social network mining algorithms comprise a local exploration of the underlying graph, which consists in referencing nodes in the neighborhood of a particular node.

The main contribution of this work is to use the community structure during the storage of large graphs that arise in social network mining. The goal is to reduce cache misses and consequently, execution time. After formalizing the problem of social network ordering as a problem of optimal linear arrangement which is known as NP-Complete, we propose NumBaCo, a heuristic based on the community structure. We present, for Katz score and Pagerank, simulations that compare classic data structures Bloc and Yale to their corresponding versions that use NumBaCo. Results on a 32-cores NUMA machine using real datasets (amazon, dblp and web-google) show that NumBaCo allows to reduce from 62% to 80% of cache misses and from 15% to 50% of execution time.

This work was initiated inside the LIRIMA Inria International Laboratory with the University of Yaoundé and Maurice Tchuenté. Those results are part of Thomas Messi Nguélé' PhD which is prepared with a Cotutelle agreement. Those results have been presented at the ParCO international conference [19] and published in the ARIMA (Revue Africaine de Recherche en Informatique et Mathématiques Appliquées) journal [3].

6.13. Run-Time Enforcement Using Büchi Games

Participants: Matthieu Renard [LaBRI], Antoine Rollet [LaBRI], Yliès Falcone.

In this work, we leverage Büchi games for the run-time enforcement of regular properties with uncontrollable events. Run-Time enforcement consists in modifying the execution of a running system to have it satisfy a given regular property, modeled by an automaton. We revisit run-time enforcement with uncontrollable events and propose a framework where we model the run-time enforcement problem as a Büchi game and synthesize sound, compliant, and optimal enforcement mechanisms as strategies. We present algorithms and a tool implementing enforcement mechanisms.We reduce the complexity of the computations performed by enforcement mechanisms at run-time by pre-computing the decisions of enforcement mechanisms ahead of time.

This work has been presented at the 24th ACM/SIGSOFT International SPIN Symposium on Model Checking of Software, SPIN 2017 [23].

6.14. GREP: Games for the Run-Time Enforcement of Properties

Participants: Matthieu Renard [LaBRI], Antoine Rollet [LaBRI], Yliès Falcone.

In this work, we developed GREP, a tool for the run-time enforcement of (timed) properties. GREP takes an execution sequence as input (stdin), and modifies it (stdout) as necessary to enforce the desired property, when possible. GREP can enforce any regular timed property described by a deterministic and complete Timed Automaton. The main novelties of GREP are twofold: It uses game theory to improve the synthesis of enforcement mechanisms, and it accounts for uncontrollable events, i.e. events that cannot be controlled by the enforcement mechanisms and thus have to be released immediately. The usability of GREP has been validated with a performance evaluation.

The associated work has been presented at the IFIP International Conference on Testing Software and Systems, ICTSS 2017 [22]

6.15. Verifying Policy Enforcers

Participants: Oliviero Riganelli [University of Milano Bicocca], Daniela Micucci [University of Milano Bicocca], Leonardo Mariani [University of Milano Bicocca], Yliès Falcone.

Policy enforcers are sophisticated run-time components that can prevent failures by enforcing the correct behavior of the software. While a single enforcer can be easily designed focusing only on the behavior of the application that must be monitored, the effect of multiple enforcers that enforce different policies might be hard to predict. So far, mechanisms to resolve interferences between enforcers have been based on priority mechanisms and heuristics. Although these methods provide a mechanism to take decisions when multiple enforcers try to affect the execution at a same time, they do not guarantee the lack of interference on the global behavior of the system. In this work we propose a verification strategy that can be exploited to discover interferences between sets of enforcers and thus safely identify a priori the enforcers that can co-exist at run-time. In our evaluation, we experimented our verification method with several policy enforcers for Android and discovered some incompatibilities.

This work has been presented at the 17-th International Conference on Run-Time Verification, RV 2017 [24].

6.16. Monitoring Decentralized Specifications

Participants: Antoine El-Hokayem, Yliès Falcone.

In this work, we define two complementary approaches to monitor decentralized systems. The first approach relies on those with a centralized specification, i.e, when the specification is written for the behavior of the entire system. To do so, our approach introduces a data-structure that i) keeps track of the execution of an automaton, ii) has predictable parameters and size, and iii) guarantees strong eventual consistency. The second approach defines decentralized specifications wherein multiple specifications are provided for separate parts of the system. We study decentralized monitorability, and present a general algorithm for monitoring decentralized specifications. We map three existing algorithms to our approaches and provide a framework for analyzing their behavior.

The associate tool THEMIS 5.1 is a framework for designing such decentralized algorithms, and simulating their behavior. This work has been presented at the 26th ACM/SIGSOFT International Symposium on Software Testing and Analysis, ISSTA 2017 [12].

6.17. Interactive Run-Time Verification - When Interactive Debugging Meets Run-Time Verification

Participants: Raphael Jakse, Yliès Falcone, Kevin Pouget, Jean-Francois Mehaut.

Run-Time Verification consists in studying a system at run-time, looking for input and output events to discover, check or enforce behavioral properties. Interactive debugging consists in studying a system at run-time in order to discover and understand its bugs and fix them, inspecting interactively its internal state. Interactive Run-Time Verification (i-RV) combines run-time verification and interactive debugging. We define an efficient and convenient way to check behavioral properties automatically on a program using a debugger. We aim at helping bug discovery and understanding by guiding classical interactive debugging techniques using run-time verification.

This work has been presented at the IEEE 28th International Symposium on Software Reliability Engineering, ISSRE 2017 [15]. It is also a part of the Nano2017 DEMA project 7.2 with STMicroelectronics.

6.18. Predictive Run-Time Verification of Timed Properties

Participants: Srinivas Pinisetty [Aalto University], Thierry Jéron [Inria Rennes], Stravos Tripakis [Aalto University], Yliès Falcone, Hervé Marchand [Inria Rennes], Viorel Preoteasa [Aalto University].

Run-Time verification (RV) techniques are used to continuously check whether the (un-trustworthy) output of a black-box system satisfies or violates a desired property. When we consider run-time verification of timed properties, physical time elapsing between actions influences the satisfiability of the property. This work introduces predictive run-time verification of timed properties where the system is not entirely a black-box but something about its behavior is known a priori. A priori knowledge about the behavior of the system allows the verification monitor to foresee the satisfaction (or violation) of the monitored property. In addition to providing a conclusive verdict earlier, the verification monitor also provides additional information such as the minimum (maximum) time when the property can be violated (satisfied) in the future. The feasibility of the proposed approach is demonstrated by a prototype implementation, which is able to synthesize predictive run-time verification monitors from timed automata.

This work has been published in the Journal of Systems and Software 2017 [6].

6.19. Concurrency-Preserving and Sound Monitoring of Multi-Threaded Component-based Systems: Theory, Algorithms, Implementation, and Evaluation

Participants: Hosein Nazarpour [Verimag], Yliès Falcone, Saddek Bensalem [Verimag], Marius Bozga [Verimag].

This work addresses the monitoring of logic-independent linear-time user-provided properties in multi-threaded component-based systems. We consider intrinsically independent components that can be executed concurrently with a centralized coordination for multiparty interactions. In this context, the problem that arises is that a global state of the system is not available to the monitor. A naive solution to this problem would be to plug in a monitor which would force the system to synchronize in order to obtain the sequence of global states at run-time. Such a solution would defeat the whole purpose of having concurrent components. Instead, we reconstruct on-the-fly the global states by accumulating the partial states traversed by the system at run-time. We define transformations of components that preserve their semantics and concurrency and, at the same time, allow to monitor global-state properties. Moreover, we present RVMT-BIP, a prototype tool implementing the transformations for monitoring multi-threaded systems described in the Behavior, Interaction, Priority (BIP) framework, an expressive framework for the formal construction of heterogeneous systems. Our experiments on several multi-threaded BIP systems show that RVMT-BIP induces a cheap run-time overhead.

This work has been published in the journal Formal Aspects of Computing 2017 [4].

6.20. Formal Analysis and Offline Monitoring of Electronic Exams

Participants: Ali Kassem [Inria Grenoble], Yliès Falcone, Pascal Lafourcade [University of Auvergne].

More and more universities are moving toward electronic exams (in short e-exams). This migration exposes exams to additional threats, which may come from the use of the information and communication technology. In this work, we identify and define several security properties for e-exam systems. Then, we show how to use these properties in two complementary approaches: model-checking and monitoring. We illustrate the validity of our definitions by analyzing a real e-exam used at the pharmacy faculty of University Grenoble Alpes (UGA) to assess students. On the one hand, we instantiate our properties as queries for ProVerif, an automatic verifier of cryptographic protocols, and we use it to check our modeling of UGA exam specifications. ProVerif found some attacks. On the other hand, we express our properties as Quantified Event Automata (QEAs), and we synthesize them into monitors using MarQ, a Java tool designed to implement QEAs. Then, we use these monitors to verify real exam executions conducted by UGA. Our monitors found fraudulent students and discrepancies between the specifications of UGA exam and its implementation.

This work has been published in the journal of Formal Methods in System Design 2017 [2].

6.21. Teaching Algorithms using Problem and Challenge Based Learning

Participant: Florent Bouchez - Tichadou.

Teaching algorithms is always a challenge at any level of the CS curriculum, as it is often viewed as a theoretical field. While many exercises revolve around classical examples that illustrate interesting algorithmic points, they are often disconnected from reality, which is a major drawback for students trying to learn. During the last four years, we have been trying to reconnect the teaching of algorithms with their applicability in the real world to M1 and L2 students, by giving them actual problems that could arise in their life of future software engineers, challenging enough to force them to use particular algorithmic techniques or data structures—e.g., linked lists, binary trees, dynamic programming or approximation algorithms.

By assigning students in groups of 5 to 6 members, we wanted to create an environment where they function as a team trying to work together to solve a problem. This allowed them to help each other in their respective comprehension, and made them more autonomous in their learning. The effective materials was provided as online pdf files so they had to read and learn from them by themselves, while the class sessions with a tutor (teacher) where used for the problem-solving part, with guidance from the tutor (who is there to make sure the learning takes place).

After four years of experimentation with M1 students, we found that the student's grades were stable, in particular there was no decrease in exams' performances compared to the classical course that was taught in the previous years. However, the students progressed in trans-disciplinary skills such a communication and the writing of essays. More importantly, students show a strong adhesion to the teaching method, 50% of them rating it as "excellent" (6) and 25% as "good" (resp. 6 and 5 on a scale from 1 (terrible) to 6 (excellent)). No student rated the course below average.

This work is still ongoing, and our plan now is to use our knowledge of the internals of compilers and run-time systems to: First, extract real-life algorithmic problems that have concrete applications; Second, create a tool that exposes the working mechanics of a running program, hence helping students to better understand how algorithms work.

7. Bilateral Contracts and Grants with Industry

7.1. Bilateral Contracts with Industry

- CORSE is involved in a contract with Kalray which objective is the automatic integration of neural networks into the manycore architecture developed by Kalray.

7.2. Bilateral Grants with Industry

- PSAIC Nano2017 is a bilateral Grant with STMicroelectronics. CORSE is involved in the development of trace analysis and hybrid compilation.
- DEMA Nano2017 is a bilateral Grant with STMicroelectronics. CORSE is involved in the development of debugging of multi-threaded applications.

8. Partnerships and Cooperations

8.1. Regional Initiatives

8.1.1. HEAVEN Persyval Project

- Title: HEterogenous Architectures: Versatile Exploitation and programiNg
- HEAVEN leaders: François Broquedis, Olivier Muller [TIMA lab]
- CORSE participants: François Broquedis, Frédéric Desprez, Georgios Christodoulis

- Computer architectures are getting more and more complex, exposing massive parallelism, hierarchically-organized memories and heterogeneous processing units. Such architectures are extremely difficult to program as they most of the time make application programmers choose between portability and performance.

  While standard programming environments like OpenMP are currently evolving to support the execution of applications on different kinds of processing units, such approaches suffer from two main issues. First, to exploit heterogeneous processing units from the application level, programmers need to explicitly deal with hardware-specific low-level mechanisms, such as the memory transfers between the host memory and private memories of a co-processor for example. Second, as the evolution of programming environments towards heterogeneous programming mainly focuses on CPU/GPU platforms, some hardware accelerators are still difficult to exploit from a general-purpose parallel application.

  FPGA is one of them. Unlike CPUs and GPUs, this hardware accelerator can be configured to fit the application needs. It contains arrays of programmable logic blocks that can be wired together to build a circuit specialized for the targeted application. For example, FPGAs can be configured to accelerate portions of code that are known to perform badly on CPUs or GPUs. The energy efficiency of FPGAs is also one of the main assets of this kind of accelerators compared to GPUs, which encourages the scientific community to consider FPGAs as one of the building blocks of large scale low-power heterogeneous multicore platforms.

  However, only a fraction of the community considers programming FPGAs for now, as configurations must be designed using low-level description languages such as VHDL that application programmers are not experienced with.

  The main objective of this project is to improve the accessibility of heterogeneous architectures containing FPGA accelerators to parallel application programmers. The proposed project focuses on three main aspects:

  – Portability: we don't want application programmers to redesign their applications completely to benefit from FPGA devices. This means extending standard parallel programming environments like OpenMP to support FPGA. Improving application portability also means leveraging most of the hardware-specific low-level mechanisms at the run-time system level ;

  – Performance: we want our solution to be flexible enough to get the most out of any heterogeneous platforms containing FPGA devices depending on specific performance needs, like computation throughput or energy consumption for example ;

  – Experiments: Experimenting with FPGA accelerators on real-life scientific applications is also a key element of our project proposal. In particular, the solutions developed in this project will allow comparisons between architectures on real-life applications from different domains like signal processing and computational finance.

  Efficient programming and exploitation of heterogeneous architectures implies the development of methods and tools for system design, embedded or not. The HEAVEN project proposal fits in the PCS research action of the PERSYVAL-lab. The PhD of Georgios Christodoulis is funded by this project.

8.1.2. AGIR DEREVES

- Title: DEcentralised Run-Time Verification and Enforcement of distributed and cyber-physical Systems
- DEREVES leader: Yliès Falcone
- CORSE participants: Yliès Falcone, Antoine El-Hokayem, Raphaël Jakse
- DEREVES aims at advancing the theory of decentralized run-time verification and enforcement for

distributed systems, with the objective of proposing realistic monitoring and monitor-synthesis algorithms for expressive specifications that can be used for the efficient monitoring of multi-threaded, distributed and cyber-physical systems. The project shall help transferring run-time verification and enforcement to a wider audience of programmers of distributed systems by providing them techniques and tools to help them guaranteeing the correctness of their systems.

8.2. National Initiatives

8.2.1. PIA ELCI

- Title: Software environment for computation-intensive applications
- Coordinator: Corinne Marchand (BULL SAS)
- CORSE participants: François Broquedis, Philippe Virouleau
- INRIA Partners: Avalon, Cardamon, Myriads; Realopt, Roma, Storm, Tadaam
- Other Partners: Algo'Tech, CEA, Cenaero, CERFACS, CORIA, Kitware, Onera, SAFRAN
- Duration: from Sept. 2014 to Sept. 2017
- Abstract: The ELCI project main goal is to develop a highly-scalable new software stack to tackle high-end supercomputers, from numerical solvers to programming environments and run-time systems. In particular, the CORSE team is studying the scalability of OpenMP run-time systems on large scale shared memory machines through the PhD of Philippe Virouleau, co-advised by researchers from the CORSE and AVALON Inria teams. This work intends to propose new approaches based on a compiler/run-time cooperation to improve the execution of scientific task-based programs on NUMA platforms. The PhD of Philippe Virouleau is funded by this project.

8.2.2. IPL ZEP

- Title: Zero-Power computing systems
- Coordinator: Kevin Marquet (INRIA Socrate)
- CORSE participants: Fabrice Rastello
- Other INRIA Partners: Cairn, Pacap
- Duration: from Apr. 2017 to Sept. 2019
- Abstract: The ZEP project addresses the issue of designing tiny computing objects with no battery by combining non-volatile memory (NVRAM), energy harvesting, micro-architecture innovations, compiler optimizations, and static analysis. The main application target is Internet of Things (IoT) where small communicating objects will be composed of this computing part associated to a low-power wake-up radio system. The ZEP project gathers four Inria teams that have a scientific background in architecture, compilation, operating system and low power together with the CEA Lialp and Lisan laboratories of CEA LETI & LIST. The major outcomes of the project will be a prototype harvesting board including NVRAM and the design of a new microprocessor associated with its optimizing compiler and operating system.

8.3. European Initiatives

8.3.1. FP7 & H2020 Projects

8.3.1.1. Mont-Blanc2

Title: Mont-Blanc (European scalable and power efficient HPC platform based on low-power embedded technology)

Program FP7

Duration: 01/10/2013 - 31/01/2017

Coordinator: Barcelona Supercomputing Center (BSC)

Mont-Blanc consortium: BSC, Bull, Arm, Juelich, LRZ, USTUTT, Cineca, CNRS, INRIA, CEA Leti, Univ. Bristol, Allinea

CORSE contact: Jean-François Méhaut

CORSE participants: Brice Videau, Kevin Pouget

The Mont-Blanc project aims to develop a European Exascale approach leveraging on commodity power-efficient embedded technologies. The project has developed a HPC system software stack on ARM, and is deployed the first integrated ARM-based HPC prototype by 2014, and is also working on a set of 11 scientific applications to be ported and tuned to the prototype system.

The rapid progress of Mont-Blanc towards defining a scalable power efficient Exascale platform has revealed a number of challenges and opportunities to broaden the scope of investigations and developments. Particularly, the growing interest of the HPC community in accessing the Mont-Blanc platform calls for increased efforts to setup a production-ready environment. The Mont-Blanc 2 project has 4 objectives:

1. To complement the effort on the Mont-Blanc system software stack, with emphasis on programmer tools (debugger, performance analysis), system resiliency (from applications to architecture support), and ARM 64-bit support
2. To produce a first definition of the Mont-Blanc Exascale architecture, exploring different alternatives for the compute node (from low-power mobile sockets to special-purpose high-end ARM chips), and its implications on the rest of the system
3. To track the evolution of ARM-based systems, deploying small cluster systems to test new processors that were not available for the original Mont-Blanc prototype (both mobile processors and ARM server chips)
4. To provide continued support for the Mont-Blanc consortium, namely operations of the original Mont-Blanc prototype, the new developer kit clusters and hands-on support for our application developers

Mont-Blanc 2 contributes to the development of extreme scale energy-efficient platforms, with potential for Exascale computing, addressing the challenges of massive parallelism, heterogeneous computing, and resiliency. Mont-Blanc 2 has great potential to create new market opportunities for successful EU technology, by placing embedded architectures in servers and HPC.

8.3.1.2. EoCoE

Title: Energy oriented Centre of Excellence for computer applications

Programm: H2020

Duration: October 2015 - October 2018

Coordinator: CEA

Partners:

Barcelona Supercomputing Center - Centro Nacional de Supercomputacion (Spain)

Commissariat A L Energie Atomique et Aux Energies Alternatives (France)

Centre Europeen de Recherche et de Formation Avancee en Calcul Scientifique (France)

Consiglio Nazionale Delle Ricerche (Italy)

The Cyprus Institute (Cyprus)

Agenzia Nazionale Per le Nuove Tecnologie, l'energia E Lo Sviluppo Economico Sostenibile (Italy)

Fraunhofer Gesellschaft Zur Forderung Der Angewandten Forschung Ev (Germany)

Instytut Chemii Bioorganicznej Polskiej Akademii Nauk (Poland)

Forschungszentrum Julich (Germany)

Max Planck Gesellschaft Zur Foerderung Der Wissenschaften E.V. (Germany)

University of Bath (United Kingdom)

Universite Libre de Bruxelles (Belgium)

Universita Degli Studi di Trento (Italy)

INRIA contact: Michel Kern

CORSE contact: Jean-François Méhaut

CORSE participants: Jean-François Méhaut, Frédéric Desprez and Francieli Zanon Boito

The aim of the present proposal is to establish an Energy Oriented Centre of Excellence for computing applications, (EoCoE). EoCoE (pronounce "Echo") will use the prodigious potential offered by the ever-growing computing infrastructure to foster and accelerate the European transition to a reliable and low carbon energy supply. To achieve this goal, we believe that the present revolution in hardware technology calls for a similar paradigm change in the way application codes are designed. EoCoE will assist the energy transition via targeted support to four renewable energy pillars: Meteo, Materials, Water and Fusion, each with a heavy reliance on numerical modeling. These four pillars will be anchored within a strong transverse multidisciplinary basis providing high-end expertise in applied mathematics and HPC. EoCoE is structured around a central Franco-German hub coordinating a pan-European network, gathering a total of 8 countries and 23 teams. Its partners are strongly engaged in both the HPC and energy fields; a prerequisite for the long-term sustainability of EoCoE and also ensuring that it is deeply integrated in the overall European strategy for HPC. The primary goal of EoCoE is to create a new, long lasting and sustainable community around computational energy science. At the same time, EoCoE is committed to deliver high-impact results within the first three years. It will resolve current bottlenecks in application codes, leading to new modeling capabilities and scientific advances among the four user communities; it will develop cutting-edge mathematical and numerical methods, and tools to foster the usage of Exascale computing. Dedicated services for laboratories and industries will be established to leverage this expertise and to foster an ecosystem around HPC for energy. EoCoE will give birth to new collaborations and working methods and will encourage widely spread best practices.

Francieli Zanon Boito started in November 2017 as post-doc for the EoCoe project. She is working with Frédéric Desprez, Thierry Deutsch (CEA INAC) and Jean-François Méhaut. Francieli is investigating the data storage issues for the scientific workflows on the nano-scale characterization center (PFNC@Minatec http://inac.cea.fr/en/Phocea/Vie_des_labos/Ast/ast_technique.php?id_ast=217).

8.3.1.3. HPC4e

Title: HPC for Energy (HPC4E), Brazil and Europe

https://hpc4e.eu

H2020 European program

2 Years Duration (December 2015 - November 2017)

H2020 program: consortium

Coordinator: Barcelona Supercomputing Center

Partners:

Centro de Investigaciones Energeticas, Medioambientales Y Tecnologicas-Ciemat (Spain)

Inria (France)

Queen Mary University of London (United Kingdom)

Iberdrola Renovables Energia (Spain)

Repsol (Spain)

Total S.A. (France)

COPPE Federal University of Rio de Janeiro (Brazil)

Laboratório Nacional Computação Cientifica (LNCC), Petropolis, (Brazil)

Instituto Technológico de Aeronautica (ITA), Brazil

Universidade Federal do Rio Grande do Sul (UFRGS), Brazil

Universidade Federal de Pernambuco (Brazil)

Petrobras (Brazil)

INRIA contact: Stephane Lanteri

CORSE particpants: Jean-François Méhaut, Frédéric Desprez, François Broquedis, Emmanuelle Saillard (Post-Doct since Dec 2016)

This project aims to apply the new exascale HPC techniques to energy industry simulations, customizing them, and going beyond the state-of-the-art in the required HPC exascale simulations for different energy sources: wind energy production and design, efficient combustion systems for biomass-derived fuels (biogas), and exploration geophysics for hydrocarbon reservoirs. For wind energy industry HPC is a must. The competitiveness of wind farms can be guaranteed only with accurate wind resource assessment, farm design and short-term micro-scale wind simulations to forecast the daily power production. The use of CFD LES models to analyze atmospheric flow in a wind farm capturing turbine wakes and array effects requires exascale HPC systems. Biogas, i.e. biomass-derived fuels by anaerobic digestion of organic wastes, is attractive because of its wide availability, renewably and reduction of CO2 emissions, contribution to diversification of energy supply, rural development, and it does not compete with feed and food feed-stock. However, its use in practical systems is still limited since the complex fuel composition might lead to unpredictable combustion performance and instabilities in industrial fuels. The next generation of exascale HPC systems will be able to run combustion simulations in parameter regimes relevant to industrial applications using alternative fuels, which is required to design efficient furnaces, engines, clean burning vehicles and power plants. One of the main HPC consumers is the oil & gas (O&G) industry. The computational requirements arising from full wave-form modeling and inversion of seismic and electromagnetic data is ensuring that the O&G industry will be an early adopter of exascale computing technologies. By taking into account the complete physics of waves in the subsurface, imaging tools are able to reveal information about the Earth's interior with unprecedented quality.

Emmanuelle Saillard was one year post-doc for the HPC4e project. She used the BOAST framework on the Alya application (BSC) and the Hou10ni application (Inria Magique 3D). Emmanuelle Saillard got an Inria Research position (CR2) in the Storm team at Bordeaux.

Two papers [18], [16] were accepted this year with the Brazilian researchers at UFRGS and also with the Magique3D team.

Jean-François Méhaut got a *Chaire* position at Laboratório Nacional Computação Cientifica (LNCC) in Petrópolis (Brazil). The LNCC is also partner of the HPC4e project. Jean-François Méhaut is working on the optimization of the MHM (Multiscale Hybrid-Mixed Methods) simulator by using the binLPT loop scheduling strategies and also new memory allocators.

8.3.1.4. PRACE-5IP

Title: PRACE-5IP (PRACE Fifht Implementation Phase)

Program H2020

Duration: 01/01/2013 - 30/04/2019

Inria partners: Hiepacs team (Inria Bordeaux Sud-Ouest), Storm team (Inria Bordeaux Sud-Ouest), Nachos team (Inria Sophia Antipolis Méditerranée), CORSE team (Inria Grenoble Rhône Alpes) INRIA contact: Stéphane Lanteri (Nachos, Sophia Antipolis)

CORSE contact: Jean-François Méhaut

CORSE participants: François Broquedis, Jean-François Méhaut

The objectives of PRACE-5IP are to build on and seamlessly continue the successes of PRACE and start new innovative and collaborative activities proposed by the consortium. These include:

- assisting the transition to PRACE2 including analysis of TransNational Access;
- strengthening the internationally recognized PRACE brand;
- continuing and extend advanced training which so far provided more than 18800 person-training days;
- preparing strategies and best practices towards Exascale computing;
- coordinating and enhancing the operation of the multi-tier HPC systems and services;
- supporting users to exploit massively parallel systems and novel architectures.

The INRIA contribution is in the prolongation of involvement (jointly with CINES) in PRACE 4IP – WP7. The participation of Inria's researchers has been enlarged to include project-teams that were all involved in the C2S@Exa Inria Project Lab. The Inria teams will contribute to the WP7 and the following sub-tasks:

- Task 7.1: Applications Enabling Services for PRACE systems
- Task 7.4 Provision of Numerical Libraries for Heterogeneous/Hybrid Architectures

The activities are organized along two complementary lines

- Generic (or transverse) technologies for simulation software
- Specific (or vertical) technologies i.e. simulation software

The CORSE activities for PRACE-5IP will start with the hiring of one year postdoc in 2018. We will work on the DIOGENEs (DisOntinous GalErkin Nanoscale Solvers) software suite developed in the Nachos team. The post-doc will investigate the new vectorization features of processors.

8.3.2. Collaborations in European Programs, Except FP7 & H2020

Program: COST

Project acronym: ArVI

Project title: Run-Time Verification beyond Monitoring

Duration: December 2014 - Dec 2018

Coordinator: Martin Leucker, University of Lubeck

Abstract: Run-Time verification (RV) is a computing analysis paradigm based on observing a system at run-time to check its expected behavior. RV has emerged in recent years as a practical application of formal verification, and a less ad-hoc approach to conventional testing by building monitors from formal specifications.

There is a great potential applicability of RV beyond software reliability, if one allows monitors to interact back with the observed system, and generalizes to new domains beyond computers programs (like hardware, devices, cloud computing and even human centric systems). Given the European leadership in computer based industries, novel applications of RV to these areas can have an enormous impact in terms of the new class of designs enabled and their reliability and cost effectiveness.

This Action aims to build expertise by putting together active researchers in different aspects of run-time verification, and meeting with experts from potential application disciplines. The main goal is to overcome the fragmentation of RV research by (1) the design of common input formats for tool cooperation and comparison; (2) the evaluation of different tools, building a growing sets benchmarks and running tool competitions; and (3) by designing a road-map and grand challenges extracted from application domains.

8.4. International Initiatives

8.4.1. Inria Associate Teams Not Involved in an Inria International Labs

8.4.1.1. IOComplexity

Title: Automatic characterization of data movement complexity

International Partner (Institution - Laboratory - Researcher):

Ohio State University (United States) - P. Sadayappan

Colorado State University (United States) - Louis-Noël Pouchet

Start year: 2015

See also: https://team.inria.fr/corse/iocomplexity/

The goal of this project is to develop new techniques and tools for the automatic characterization of the data movement complexity of an application. The expected contributions are both theoretical and practical, with the ambition of providing a fully automated approach to I/O complexity characterization, in stark contrast with all known previous work that are strictly limited to pen-and-paper analysis.

I/O complexity becomes a critical factor due in large part to the increasing dominance of data movement over computation in energy consumption for current and emerging architectures. This project aims at enabling: 1. the selection of algorithms according to this new criteria (as opposed to the criteria on arithmetic complexity that has been used up to now); 2. the design of specific architectures in terms of cache size, memory bandwidth, GFlops etc. based on application-specific bounds on memory traffic; 3. higher quality feedback to the user, the compiler, or the run-time system about data traffic, a major performance and energy factor.

8.4.1.2. PROSPIEL

- Title: Profiling and specialization for locality
- International Partner (Institution - Laboratory - Researcher):

  Universidade Federal de Minas Gerais (Brazil) - Computer Science Department - Fernando Magno Quintão Pereira
- Start year: 2015
- See also: https://team.inria.fr/alf/prospiel/
- The PROSPIEL project aims at optimizing parallel applications for high performance on new throughput-oriented architectures: GPUs and many-core processors. Traditionally, code optimization is driven by a program analysis performed either statically at compile-time, or dynamically at run-time. Static program analysis is fully reliable but often over-conservative. Dynamic analysis provides more accurate data, but faces strong execution time constraints and does not provide any guarantee. By combining profiling-guided specialization of parallel programs with run-time checks for correctness, PROSPIEL seeks to capture the advantages of both static analysis and dynamic analysis. The project relies on the polytope model, a mathematical representation for parallel loops, as a theoretical foundation. It focuses on analyzing and optimizing performance aspects that become increasingly critical on modern parallel computer architectures: locality and regularity.

8.4.2. Participation in Other International Programs

- EnergySFE (STIC-Amsud)
  - Leader: University Federal of Santa Catarina (UFSC): Màrcio Castro
  - Partners: UFSC (Florianapolis, Brazil), UFRGS (Porto Alegre, Brazil), ESPE (Ecuador), CNRS (LIG/CORSE, TIMA, LSPSC)
  - http://energysfe.ufsc.br/
  - Duration: January 2016 - December 2017
  - CORSE participants: Jean-François Méhaut, François Broquedis, Frédéric Desprez
  - The main goal of the EnergySFE research project is to propose fast and scalable energy-aware scheduling and fault tolerance techniques and algorithms for large-scale highly parallel architectures. To achieve this goal, it will be crucial to answer the following research questions:

* How to schedule tasks and threads that compete for resources with different constraints while considering the complex hierarchical organization of future Exascale supercomputers?
* How to tolerate faults without incurring in too much overhead in future Exascale supercomputers?
* How scheduling and fault tolerance approaches can be adapted to be energy-aware?

The first EnergySFE workshop was organized by the CORSE team at the INRIA Minatec building in September 2016.

8.5. International Research Visitors

8.5.1. Visits of International Scientists

- Julien Langou (UCDenver) is visiting professor from September 2016 till July 2017
- Henrique Cota de Freitas (PUC Minas) visited the team for a week in April 2017 (Pedro Penna's thesis)
- Philippe Navaux (UFRGS) visited the team for a week in February 2017. (HPC4e project)
- Paolo Rech (UFRGS) visited the team for a week in September 2017 (EnergySFE project).
- Mohamad Jaber (American University of Beirut, Lebanon) visited the team for a week in January 2017.
- Maurice Tchuente (Yaoundé 1) visited the team for a week in June 2017 (related to Thomas Messi Nguele's thesis).
- Márcio Castro (UFSC) visited the team for two weeks in February 2017 (EnergySFE project).
- Laercio Pilla (UFSC) visited the team for a week in December 2017 (EnergySFE project).

8.5.2. Visits to International Teams

- Jean-François Méhaut visited for one week (July 2017) the UFRGS (Porto Alegre) and the GPPD group for the HPC4e project.
- Jean-François Méhaut visited for one week (July 2017) the Federal University of Rio de Janeiro for the HPC4e project.
- Jean-François Méhaut visited for one day (July 2017) the LNCC to prepare the research work for the chaire position and also for the HPC4e project.
- Jean-François Méhaut visited for a week (August 2017) the LaPeSD and ECL laboratories at UFSC (Florianopolis). He was member of the master jurie of Pedro Penna. This visit was funded by the EnergySFE project.
- Jean-François Méhaut visited for one week (August 2017) the PUC Minas to prepare the cotutelle agreement of the Pedro Penna's PhD. This agreement is signed between PUC Minas, LIG, Ecole Doctorale MSTII, Post-Graduation program of PUC Minas and the COMUE Grenoble Alpes.
- Jean-François Méhaut visited for one day (December 2017) the French consulate in Rio de Janeiro and the CNRS Bureau. He presented the first results of the research work at LNCC.

8.5.2.1. Sabbatical programme

- Fabrice Rastello is on sabbatical at Colorado State University (USA) from July 2017 till July 2018

8.5.2.2. Research Stays Abroad

- Jean-François Méhaut holds a *Chaire* position at Laboratório Nacional Computação Cientifica (LNCC) in Petrópolis (Brazil). This *Chaire* position is funded by the LNCC and the French Consulate in Rio de Janeriro.

9. Dissemination

9.1. Promoting Scientific Activities

9.1.1. Scientific Events Organisation

9.1.1.1. General Chair, Scientific Chair

- Fabrice Rastello: General Chair "Journées française de la compilation", Lyon, June 2017

9.1.1.2. Member of the Organizing Committees

- Fabrice Rastello: Steering Committee ACM/IEEE CGO; Steering Committee "Journées française de la compilation"
- Yliès Falcone: Publicity Chair of the 24th International SPIN Symposium on Model Checking of Software

9.1.2. Scientific Events Selection

9.1.2.1. Chair of Conference Program Committees

- Fabrice Rastello: Program Chair "Journées française de la compilation", Lyon, June 2017
- Yliès Falcone: Track Chair on Software Verification and Testing at the 2017 ACM Symposium on Applied Computing

9.1.2.2. Member of the Conference Program Committees

- Fabrice Rastello: ACM/IEEE CGO'18
- François Broquedis: IEEE IPDPS'18
- Jean-François Méhaut: IEEE IPDPS'18
- Frédéric Desprez: ACM/SIGSIM HPC'17, ACM/SIGARCH HPDC'17, IEEE/ACM ISFEC'17, IEEE IPDS'17, IEEE ICDCS'17, IEEE ICA3PP'17, Special Track: Vision/Blue Sky Thinking, EBDMA'17, Europar'17, ICPADS'17, Closer 2017
- Yliès Falcone: CRI'17, MSR'17, RV-CuBES, RV'17, RW-BRMS'17, TASE 2017, iFM 2017, PDP 2017, DATE 2017 – Topic E3

9.1.3. Journal

9.1.3.1. Reviewer - Reviewing activities

- Frédéric Desprez: IJHPCA
- Yliès Falcone: ACM Transactions on Software Engineering and Methodology (TOSEM), Formal Aspects of Computing, ACM Transactions on Automatic and Control, Acta Informatica, Formal Methods in System Design

9.1.4. Invited talks

- Frédéric Desprez: Entretiens Jacques Cartier, Montréal, Oct. 18 2017 "From IoT Devices to Cloud Computing Infrastructures"

9.1.5. Scientific expertise

- Frédéric Desprez: European project in the FP7 framework; Comité d'orientation stratégique de CIRRUS (COMUE Paris); Groupe Technique GENCI; GENCI, expert for grants of computing resources (CT6); COFECUB - CAPES 2018.
- Yliès Falcone: Representative of France in the COST Action ARVI
- Yliès Falcone: COST Action ARVI, co-leader of Working Group on Core Run-Time Verification
- Jean-François Méhaut: Eurolab-4-HPC, expert for cross site mobility research grants
- Jean-François Méhaut: GENCI, expert for grants of computing resources (CT6)

- Jean-François Méhaut: GENCI, reviewer for C3I (*Certificat de Compétences en Calcul Intensif*)

9.1.6. Research administration

- Frédéric Desprez: Deputy Scientific Director at INRIA
- Frédéric Desprez: Director of the GIS GRID5000
- Frédéric Desprez: Conseil Scientifique ESIEE Paris
- Yliès Falcone: Mission Valorisation for Laboratoire d'Informatique de Grenoble

9.2. Teaching - Supervision - Juries

9.2.1. Teaching

Master II: Fabrice Rastello, Advanced Compilers, 12 hours, ENS Lyon

Master I: Jean-François Méhaut, Operating System Design, 50 hours, Polytech Grenoble

L3: Jean-François Méhaut, Numerical Methods, 50 hours, Polytech Grenoble,

L3: Jean-François Méhaut, Advanced Algorithms, 50 hours, Polytech Grenoble

Master I: Jean-François Méhaut, Parallel Algorithms and Programming, 10 hours (M1 Informatique), UFR IM2AG, Université Grenoble Alpes

L3: François Broquedis, Imperative programming using python, 40 hours, Grenoble Institute of Technology (Ensimag)

L3: François Broquedis, C programming, 80 hours, Grenoble Institute of Technology (Ensimag)

M1: François Broquedis, Operating systems and concurrent programming, 40 hours, Grenoble Institute of Technology (Ensimag)

M1: François Broquedis, Operating Systems Development Project - Fundamentals, 20 hours, Grenoble Institute of Technology (Ensimag)

M1: François Broquedis, Operating Systems Project, 20 hours, Grenoble Institute of Technology (Ensimag)

Master: Florent Bouchez Tichadou, Compilation project, 20 hours, M1 Info & M1 MoSIG

Licence: Florent Bouchez Tichadou, C programming, 20 hours, L3, Grenoble Institute of Technology (Ensimag)

Licence: Florent Bouchez Tichadou, Introduction to Programming, 24 hours, L1 UGA

Master: Florent Bouchez Tichadou, Algorithmic Problem Solving, 41 hours, M1 MoSIG

Licence: Florent Bouchez Tichadou, Algorithms languages and programming, 111 hours, L2 UGA

Licence: Florent Bouchez Tichadou is responsible of the second year of INF (informatique) and MIN (mathématiques et informatique) students at UGA

Master I: Yliès Falcone Proof Techniques and Logic Reminders, MoSIG, 3 hours

Master I: Yliès Falcone Recaps on Object-Oriented Programming, MoSIG, 3 hours

Master I: Yliès Falcone Programming Language Semantics and Compiler Design, MoSIG and Master informatique, 96 hours

License: Yliès Falcone Languages and Automata, UJF, 105 hours

Master: Yliès Falcone is co-responsible of the first year of the International Master of Computer Science (Univ. Grenoble Alpes and INP ENSIMAG)

Master I: Frédéric Desprez, Parallel Algorithms and Programming, 30 hours (MOSIG and Info)

9.2.2. Supervision

PhD defended: Thomas Gonçalves, Contributions à la parallélisation de méthodes de type transport Monte-Carlo, defended on September 28 2017, advised by Marc Perache (CEA/DAM), Frédéric Desprez, and Jean-François Méhaut

PhD defended: Vanessa Vargas, Approche logicielle pour améliorer la fiabilité d'applications parallèles implémentées sur des processeurs multi-cœurs et many-cœurs, defended on April 28 2017, advised by Raoul Velazco (CNRS, TIMA), and Jean-François Méhaut

PhD defended: Hosein Nazarpour, Monitoring Distributed and Multi-threaded Component-Based Systems, defended on June 26, 2017, advised by Yliès Falcone and Saddek Bensalem (Verimag).

PhD defended: Matthieu Renard, Run-Time Enforcement of (Timed) Properties with Uncontrollable Events, defended on December 11, 2017, advised by Yliès Falcone, Antoine Rollet and Mohamed Mosbah (University of Bordeaux).

PhD defended: Pedro Silva, On the mapping of distributed applications on multiple clouds, defended on December 11 2017, advised by Frederic Desprez, C. Perez (INRIA, Avalon team)

PhD in progress: François Gindraud, Semantics and compilation for a data-flow model with a global address space and software cache coherency, January 1st 2013, advised by Fabrice Rastello and Albert Cohen.

PhD in progress: Antoine El-Hokayem, Decentralised and Distributed Monitoring of Cyber-Physical Systems, October 2017, advised by Yliès Falcone.

PhD in progress: Fabian Grüber, Interactive & iterative performance debugging, September 2016, advised by Fabrice Rastello and Yliès Falcone.

PhD in progress: Georgios Christodoulis, Adaptation of a heterogeneous run-time system to efficiently exploit FPGA, October 2015, advised by Frederic Desprez, Olivier Muller (TIMA/SLS), and François Broquedis

PhD in progress: Luis Felipe Millani, Auto-tuning for optimizations of performance and power consumption, November 2015, advised by Lucas Schnoor (UFRGS) and Jean-François Méhaut

PhD in progress: Philippe Virouleau, Improving the performance of task-based run-time systems on large scale NUMA machines, March 2015, advised by Thierry Gautier (INRIA/AVALON), Fabrice Rastello, and François Broquedis

PhD in progress: Raphaël Jakse, Monitoring and Debugging Component-Based Systems, October 2016, advised by Jean-François Méhaut and Yliès Falcone.

PhD in progress: Thomas Messi Nguelé, Domain Specific Languages for Social Networks Analysis on Multi-Core Architectures, October 2014, advised by Maurice Tchuenté (Yaoundé I, LIRIMA) and Jean-François Méhaut

PhD in progress: Ye Xia, Scaling and placement for autonomic management of elasticity of applications in a widely distributed cloud, November 2015, advised by Thierry Coupaye (Orange), Frédéric Desprez, and Xavier Etchevers (Orange)

PhD in progress: Pedro Henrique Penna, Towards an Operating System for Manycore Platforms, October 2017, advised by Marcio Castro (UFSC), François Broquedis, Henrique Cota de Freitas (PUC Minas) and Jean-François Méhaut

9.2.3. Juries

9.2.3.1. Frédéric Desprez

- Nelson Lossing, reviewer, *Compilation pour machines à mémoire réparties: une approche multi-passe*, PhD, Université de recherche Paris Science, April 3 2017
- Luis Pineda, reviewer, *Efficient Support for Data-Intensive Workflows on Geo-Distributed Clouds*, Université de Rennes, May 24 2017
- Adrien Lebre, member of the committee, *Contributions to Large-scale Distributed Systems The infrastructure Viewpoint*, Nantes, September 1 2017

- Thomas Gonçalves, Advisor with Jean-François Méhaut and Marc Pérache (CEA DAM), *Contributions à la parallélisation de méthodes de type transport Monte-Carlo*, PhD Université de Grenoble Alpes, September 28 2017
- Pierre Ramet, reviewer, *Heterogeneous architectures, Hybrid methods, Hierarchical matrices for Sparse Linear Solvers*, Université de Bordeaux, November 27 2017
- Pedro Silva, advisor with Christian Perez (Avalon), *On the mapping of distributed applications onto multiple Clouds*, ENS Lyon, December 11 2017
- Millian Poquet, chair, *Approche par la simulation pour la gestion de ressources*, Université de Grenoble Alpes, December 19 2017

9.2.3.2. Jean-François Méhaut

- Soraya Zertal, Reviewer, *Contributions to data storage systems: modelling, simulation and evaluation tools*, HDR Université de Versailles, November 2017
- Abdou Guermouche, Reviewer, *Towards Efficient Sparse Direct Solvers for Modern High-Performance Architectures*, HDR Université de Bordeaux, December 2017
- Vanessa Vargas, Advisor with Raoul Velzco (TIMA), *Approche logicielle pour améliorer la fiabilité d'applications parallèles implémentées sur des processeurs multi-cœurs et many-cœurs*, PhD Université de Grenoble Alpes, April 2017
- Thomas Gonçalves, Advisor with Marc Pérache (CEA DAM) and Frédéric Desprez, *Contributions à la parallélisation de méthodes de type transport Monte-Carlo*, PhD Université de Grenoble Alpes, September 2017
- Krishna Singh, Advisor with Stéphane Redon (LJK, Nano-D), *Algorithmes pour la dynamique moléculaire restreinte de manière adaptative*, PhD Université de Grenoble Alpes, November 2017

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Publications of the year

Articles in International Peer-Reviewed Journals

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[16] J. LUCA BEZ, F. ZANON BOITO, L. M. SCHNORR, P. O. NAVAUX, J.-F. MÉHAUT. *TWINS: Server Access Coordination in the I/O Forwarding Layer*, in "25th Euromicro International Conference on Parallel, Distributed and Networked-based Processing", St. Petersburg, Russia, I. KOTENKO, Y. COTRONIS, M. DANESHTALAB (editors), Proceedings of the 25th Euromicro International Conference on Parallel, Distributed and Network-based Processing (PDP), IEEE Xplore Digital Library, March 2017, https://hal.archives-ouvertes.fr/hal-01515047

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