RESEARCH CENTRE

Grenoble - Rhône-Alpes

IN PARTNERSHIP WITH:

Institut national des sciences appliquées de Lyon

2020 ACTIVITY REPORT

Project-Team SOCRATE

Software and Cognitive radio for telecommunications

IN COLLABORATION WITH: Centre of Innovation in Telecommunications and Integration of services

DOMAIN

Networks, Systems and Services, Distributed Computing

THEME

Networks and Telecommunications

Contents

Project-Team SOCRATE

Creation of the Team: 2012 January 01, updated into Project-Team: 2013 July 01

Keywords

Computer sciences and digital sciences

A1.1.2. – Hardware accelerators (GPGPU, FPGA, etc.)

A1.1.10. – Reconfigurable architectures

A1.1.12. – Non-conventional architectures

A1.2.5. – Internet of things

A1.2.6. – Sensor networks

A1.5.2. – Communicating systems

A2.3.1. – Embedded systems

A2.6.1. – Operating systems

A5.9. – Signal processing

A8.6. – Information theory

Other research topics and application domains

B6.2. – Network technologies

B6.2.2. – Radio technology

B6.4. – Internet of things

B6.6. – Embedded systems

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2 Overall objectives

2.1 Introduction

The success of radio networking relies on a small set of rules: *i)* protocols are completely defined beforehand, *ii)* resource allocation policies are mainly designed in a static manner and *iii)* access network architectures are planned and controlled. Such a model obviously lacks adaptability and also suffers from a suboptimal behavior and performance.

Because of the growing demand for radio resources, several heterogeneous standards and technologies have been introduced by the standard organizations or industry by different workgroups within the IEEE

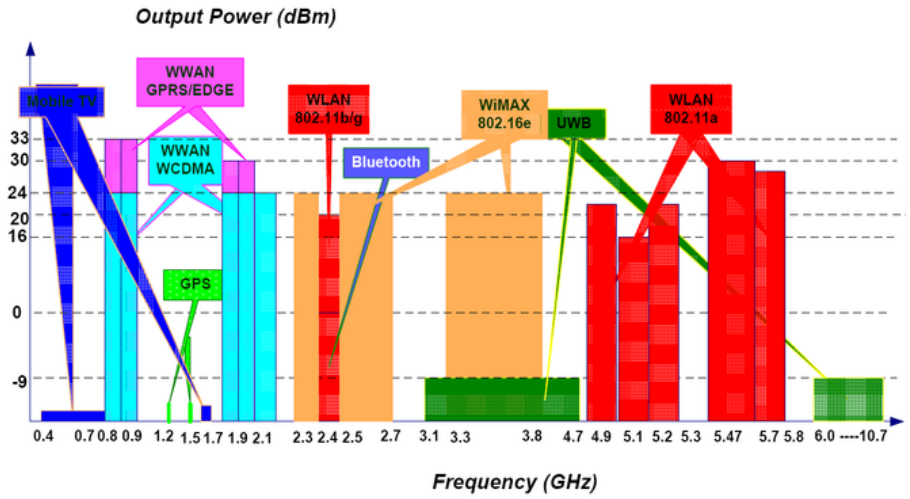

Figure 1: The most recent standards for wireless communications are developed in the UHF and VHF bands. These bands are mostly saturated *(source: WPAN/WLAN/WWAN Multi-Radio Coexistence, IEEE 802 Plenary, Atlanta, USA, Nov.2007)*

(802 family), ETSI (GSM), 3GPP (3G, 4G) or the Internet Society (IETF standards) leading to the almost saturated usage of several frequency bands (see Fig. 1).

These two facts, obsolescence of current radio networking rules on one hand, and saturation of the radio frequency band on the other hand, are the main premises for the advent of a new era of radio networking that will be characterized by self-adaptive mechanisms. These mechanisms will rely on software radio technologies, distributed algorithms, end-to-end dynamic routing protocols and therefore require a cross-layer vision of "cognitive wireless networking": *Getting to the meet of Cognition and Cooperation, beyond the inherent communication aspects: cognition is more than cognitive radio and cooperation is not just relaying. Cognition and cooperation have truly the potential to break new ground for mobile communication systems and to offer new business models.* [33]

From a social perspective, pervasive communications and ambient networking are becoming part of more and more facets of our daily life. Probably the most popular usage is mobile Internet access, which is made possible by numerous access technologies, e.g. cellular mobile networks, WiFi, Bluetooth, etc. The access technology itself is becoming *transparent for the end user*, who does not care about how to access the network but is only interested in the services available and in the quality of this service.

Beyond simple Internet access, many other applications and services are built on the basis of pervasive connectivity, for which the communication is just a mean, and not a finality. Thus, the wireless link is expected to even be *invisible to the end user* and constitutes the first element of the Future Internet of Things [32], to develop a complete twin virtual world fully connected to the real one.

The way radio technologies have been developed until now is far from offering a real wireless convergence [22]. The current development of the wireless industry is surely slowed down by the lack of radio resources and the lack of systems flexibility.

One can get rid of this technological bottleneck by solving three complementary problems: *terminal flexibility, agile radio resource management* and *autonomous networking*. These three objectives are subsumed by the concept of *Software Radio*, a term coined by J. Mitola in his seminal work during the early 90's [30, 29]. While implementing everything in software nodes is still an utopia, many architectures now hitting the market include some degree of programmability; this is called Software-Defined Radio. The word "defined" has been added to distinguish from the ideal software radio. A software *defined* radio is a software radio which is defined for a given frequency range and a maximal bandwidth.

In parallel, the development of new standards is threatened by the radio spectrum scarcity. As illustrated in Fig. 1, the increasing number of standards already causes partial saturation of the UHF band, and will probably lead to its full saturation in the long run. However, this saturation is only

"virtual" because all equipments are fortunately not emitting all the time [22]. A good illustration is the so-called "white spaces", i.e. frequency bands that are liberated by analog television disappearing and can be re-used for other purposes, different rules are set up in different countries. In this example, a solution for increasing the real capacity of the band originates from *self-adaptive behavior*. In this case, flexible terminals will have to implement agile algorithms to share the radio spectrum and to avoid interference. In this context, cooperative approaches are even more promising than simple resource sharing algorithms.

With Software-Defined Radio technology, terminal flexibility is at hand, many questions arise that are related to the software layer of a software radio machine: how will this kind of platform be programmed? How can we write programs that are portable from one terminal to another? Autonomous networking will only be reached after a deep understanding of network information theory. Thus, given that there will be many ways for transmitting data from one point to another, what is the most efficient way in terms of throughput? power consumption? etc. Last but not least, agile Radio Resource sharing is addressed by studying MIMO (multiple-input and multiple-output) and multi-standard radio front-end. This new technology is offering a wide range of research problems. These three topics: software programming of a software radio machine, distributed algorithms for radio resource management and multi-standard radio front-end have constituted the research directions of Socrate at its creation.

2.2 Technological State of the Art

A Software-Defined Radio (SDR) system is a radio communication system in which computations that in the past were typically implemented in hardware (e.g. mixers, filters, amplifiers, modulators/demodulators, detectors, etc.) are instead implemented as software programs [30, 25].

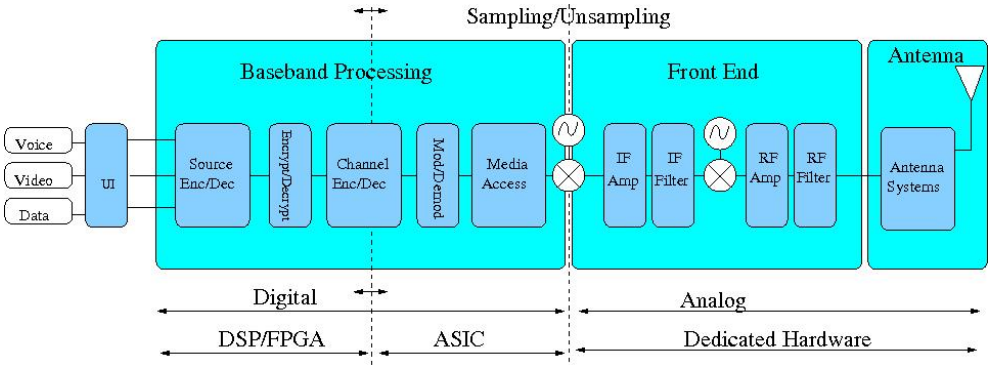

Figure 2: Radio Block Diagram, highlighting separation between digital and analog parts, as well as programmable, configurable and fixed hardware parts.

SDR Technology The different components of a radio system are illustrated in Fig. 2. Of course, all of the digital components may not be programmable, but the bigger the programmable part (DSP/FPGA part on Fig. 2), the more *software* the radio. Dedicated IPs[1] are needed, for these IP it is more suitable to use the term *configurable* than programmable. In a typical SDR, the analog part is limited to a frequency translation down to an intermediate band which is sampled and all the signal processing is done digitally.

SDR Forum Classification To encourage a common meaning for the term "SDR" the SDR Forum (renamed *Wireless Innovation Forum* (`http://www.wirelessinnovation.org`) proposes to distinguish five tiers:

- *Tier 0 – Hardware Radio:* The radio parameters cannot be changed, radio is implemented only with hardware components.

[1] In this context, IP stand for *Intellectual Properties, this term is widely used to designated dedicated special-purpose circuit blocks implemented in various technologies: Asic,* FPGA, DSP, *etc.*

- *Tier 1 – Software Controlled Radio:* A radio where only the control functions are implemented in software, baseband processing is still performed in hardware, the radio is able to switch between different hardware.
- *Tier 2 – Software-Defined Radio:* The most popularly understood definition of SDR: the radio includes software control of modulation, bandwidth, frequency range and frequency bands. Conversion to digital domain still occurs after frequency conversion. It is currently implemented using a wide range of technologies: Asics, FPGAs, DSPs, etc.
- *Tier 3 – Ideal Software Radio:* Digital conversion occurs directly at the antenna, programmability extends to the whole system.
- *Tier 4 – Ultimate Software Radio:* Same reconfigurability capabilities as in Tier 3, but with a switching between two configurations in less than one millisecond.

The main restriction to build an ideal software radio is sampling rate: sampling at a high rate is not an easy task. Following the Shannon-Nyquist theorem, sampling the RF signal at a rate greater than twice the frequency of the signal is sufficient to reconstruct the signal. Sampling can be done at lower rate (decimation), but errors can be introduced (aliasing) that can be corrected by filtering (dirty radio concept). Building an SDR terminal implies a trade-of between sampling frequency and terminal complexity. For instance, sampling at 4.9 GHz would require a 12-bit resolution ADC with at least 10GHz sample rate which is today not available with reasonable power consumption (several hundreds Watt).

Cognitive Radio SDR technology enables *over the air programming* (Otap) which consists in describing methods for distributing new software updates through the radio interface. However, as SDR architectures are heterogeneous, a standard distribution method has not emerged yet.

Cognitive Radio is a wireless communication system that can sense the air, and decide to configure itself in a given mode, following a local or distributed decision algorithm. Although Tier 3 SDR would be an ideal platform for cognitive radio implementation, cognitive radios do not have to be SDR.

Cognitive Radio is currently a very hot research topic as show the dozens of sessions in research conferences dedicated to it. In 2009, the American National Science Foundation (NSF) held a workshop on "Future Directions in Cognitive Radio Network Research" [31]. The purpose of the workshop was to explore how the transition from cognitive radios to cognitive radio *networks* can be made. The resulting report indicated the following:

- Emerging cognitive radio technology has been identified as a high impact disruptive technology innovation, that could provide solutions to the *radio traffic jam* problem and provide a path to scaling wireless systems for the next 25 years.
- Significant new research is required to address the many technical challenges of cognitive radio networking. These include dynamic spectrum allocation methods, spectrum sensing, cooperative communications, incentive mechanisms, cognitive network architecture and protocol design, cognitive network security, cognitive system adaptation algorithms and emergent system behavior.

The report also mentioned the lack of cognitive radio testbeds and urged *"The development of a set of cognitive networking test-beds that can be used to evaluate cognitive networks at various stages of their development"*, which, in some sense strengthens the creation of the Socrate team and its involvement in the FIT project [27].

3 Research program

3.1 Flexible Radio Front-End

This axis mainly deals with the radio front-end of software radio terminals. In order to ensure a high flexibility in a global wireless network, each node is expected to offer as many degrees of freedom as possible. For instance, the choice of the most appropriate communication resource (frequency channel,

spreading code, time slot,...), the interface standard or the type of antenna are possible degrees of freedom. The *multi-** paradigm denotes a highly flexible terminal composed of several antennas providing MIMO features to enhance the radio link quality, which is able to deal with several radio standards to offer interoperability and efficient relaying, and can provide multi-channel capability to optimize spectral reuse. On the other hand, increasing degrees of freedom can also increase the global energy consumption, therefore for energy-limited terminals a different approach has to be defined.

In this research axis, we expect to demonstrate optimization of flexible radio front-end by fine grain simulations, and also by the design of home made prototypes. Of course, studying all the components deeply would not be possible given the size of the team, we are currently not working in new technologies for DAC/ADC and power amplifiers which are currently studied by hardware oriented teams. The purpose of this axis is to build system level simulation taking into account the state of the art of each key component.

3.2 Software Radio Programming Model

This research research axis is concerned with embedded software aspect for low power embedded systems: how can they be adapted to integrate some reconfigurability.

The expected contributions of Socrate in this research axis are :

- The design and implementation of a software tools for embedded systems and ultra-low power sensor.
- Prototype implementations of novel transiently powered devices.
- Development of *smart nodes*: a low-power wireless sensor adapted to WSN (Wireless Sensor Network) applications and possibly without battery.
- Methodology clues and programming tools to program all these prototypes.

3.3 Evolution of the Socrate team

In 2018 the Socrate team which was originaly conceived to develop software defined radio has decided to split in two teams: the Maracas team (https://team.inria.fr/maracas/) was created with what consisted former Socrate Axis 2 : "Multi-User Communications and Agile Radio Ressource Sharing". Maracas is directed by Jean-Marie Gorce, and the Socrate team now consists in two research axis (described above) which were the Axis 1 and 3 previous version of Socrate.

The advent of non-volatile memory technologies (NVRAM) is causing a major evolution in all software layers. On the one hand, the non-volatility of data is a nice solution to memory inconsistencies that occur, for instance, on a power outage. On the other hand, these memories have very different performances from the usual DRAM, which tends to the appearance of hybrid and complex memory hierarchies. Many technological and scientific challenges are to be faced in all software layers to deal with these two sets of issues.

During two years, Socrate worked within the framework of very low consumption sensors and devices either on the radio side or on the embedded systems side, trying to study what could be next generation sensors powered by harvesting energy from their environnement. The Socrate team proposed, with Sytare [23], a software solution allowing to develop embedded applications on platforms supporting an intermittent power supply and integrating NVRAM. The IPL ZEP (https://project.inria.fr/iplzep/) was also launched by Socrate in 2018 to respond to various scientific challenges related to this issue.

However this research direction seems too fragile to really build a complete Inria project on it. The banckrupty of start-up eVaderis with which Socrate had a PhD defended [26], together with the small energy quantities gathered by non-solar energy harvesting are signs of this weakness. It is probably to early to start, as we wished, a research team on battery-free next generation sensors. We finally decided to stop Socrate and to continue on various research team projects.

The evolution predicted for the Socrate team is represented on Fig. 3. As mentioned before, we do not plan to ask for the renewal of Socrate as an Inria project team, so Socrate should probably be ended by the end of 2021. In addition to the creation of the Maracas Inria project team headed by Jean-Marie

Gorce (1st July 2018), two members (Tanguy Risset and Florent de Dinechin) are involved in the creation of a project-team, named *Emeraude*, focused on a new topic: embedded programmable audio systems in collaboration with Grame-CNCM (https://www.grame.fr/recherche). The other members are involved in teams that will not give rise to new Inria teams: Kevin Marquet and Guillaume Salagnac are involved in the creation of a Team called Phenix targeting digital ecological transition, and Florin Hutu and Guillaume Villemaud will continue to study low power radio tansceiver in close collaboration with Ampere laboratory in Lyon.

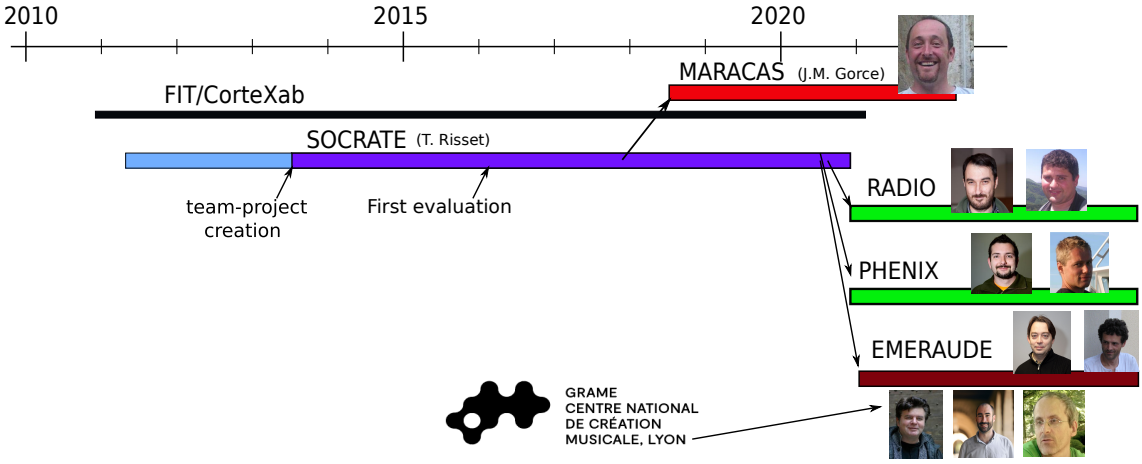

Figure 3: Evolution of the Socrate team members

4 Application domains

Here are the relevant research domains where Socrate efforts are useful:

- Antennas and RF Front-Ends: This is a key issue for reducing interference, increasing capacity and reusing frequency. Hot topics such as wake-up radio or multi protocol parallel radio receivers are directly impacted by research on Antennas. Socrate has research work going on in this area.
- Wake-up radio. In the context of transiently powered systems, wake-up radio is still a hot topic rather studied by micro-electronics laboratories (CEA Leti for instance). Socrate have been studied a particular prototype for many years.
- Software stack for transiently powered sensor. Battery-free sensor are foreseen as a major technological evolution for next IoT generation. Surviving power outage is a new challenge for sensors. Socrate has been one of the first team to work on that topic.
- High level tools for FPGA programming. With the end of Moore low, FPGA are seen as the opportunity to continue performance growth. The acquisition of Altera by Intel and, more recently, of Xilinx by AMD is a clear sign of it. Socrate is studying arithmetic operator on FPGA as well as high level compilation flow for FPGA.

5 Highlights of the year

- In [7] was presented the first formal modeling and proof (with Coq) of a transiently powered system. This result highlights the bridge between architecture design and formal proof validation that could be realized within Inria.
- The publication in IEEE Wireless communication [6] highlights the outcomes of many years of research on full duplex systems in Socrate

- The publication in ACM Taco [5] together with the hiring of our former PhD student Yohann Uguen at Intel/Altera (UK) and the recent temporary leave of Luc Forget at Xilinx (USA) illustrate the growing influence of Socrate in FPGA tool design.

6 New software and platforms

6.1 New software

6.1.1 FloPoCo

Name: Floating-Point Cores, but not only

Keyword: Synthesizable VHDL generator

Functional Description: The purpose of the open-source FloPoCo project is to explore the many ways in which the flexibility of the FPGA target can be exploited in the arithmetic realm.

URL: http://flopoco.gforge.inria.fr/

Authors: Florent de Dinechin, Bogdan Pasca, Jérémie Detrey, Radu Marius Tudoran, Sebastian Banescu, Caroline Collange, Cristian Klein-Halmaghi, Miora Maria Joldes, Xavier Pujol

Contact: Florent de Dinechin

Participants: Florent de Dinechin, Luc Forget

Partners: CNRS, ENS Lyon, UCBL Lyon 1, UPVD

6.1.2 Sytare

Keywords: Embedded systems, Operating system, Non volatile memory

Functional Description: Sytare is an embedded operating system targeting tiny platforms with intermittent power. In order to make power failures transparent for the application, the system detects imminent failures and saves a checkpoint of program state to non-volatile memory. Hardware peripherals are also made persistent without requiring developer attention.

URL: https://gitlab.inria.fr/citi-lab/sytare

Publication: hal-01460699

Authors: Tristan Delizy, Gautier Berthou, Guillaume Salagnac, Kevin Marquet, Tanguy Risset

Contact: Guillaume Salagnac

6.1.3 NanoTracer

Name: NanoTracer

Keywords: Embedded systems, Power monitoring, Low power consumption

Functional Description: NanoTracer is a high performance ammeter dedicated to power measurements for small devices. The system measures currents between 100nA and 100mA (gain is audo-adjusted dynamically) with a sampling frequency of 2Msps. Data is streamed to a PC over USB which enables long-running experiments, or just real-time visualization of data.

URL: https://geromueller.de/nanotracer/

Contacts: Guillaume Salagnac, Tanguy Risset

6.1.4 marto

Name: Modern Arithmetic Tools

Keywords: High-level synthesis, Arithmetic, FPGA

Functional Description: Marto provides C++ headers to implement custom sized arithmetic operators such as:

Custom sized posits and their environment (including the quire) Custom sized IEEE-754 numbers Custom sized Kulisch accumulators (and sums of products)

URL: https://gitlab.inria.fr/lforget/marto

Publication: hal-02130912v4

Contacts: Yohann Uguen, Luc Forget, Florent de Dinechin

Participants: Yohann Uguen, Florent de Dinechin, Luc Forget

6.1.5 hint

Name: High-level synthesis Integer Library

Keyword: High-level synthesis

Functional Description: Hint is an header-only arbitrary size integer API with strong semantics for C++. Multiple backends are provided using various HLS libraries, allowing a user to write one operator and synthetize it using the main vendor tools.

URL: https://github.com/yuguen/hint

Publication: hal-02131798v2

Contacts: Yohann Uguen, Luc Forget, Florent de Dinechin

Participants: Yohann Uguen, Florent de Dinechin, Luc Forget

6.1.6 Syfala

Name: Low-Latency Synthesizer on FPGA

Keywords: FPGA, Compilers, High-level synthesis, Audio signal processing

Functional Description: The goal of Syfala is to design an FPGA-based platform for multichannel ultra-low-latency audio Digital Signal Processing programmable at a high-level with Faust and usable for various applications ranging from sound synthesis and processing to active sound control and artificial sound field/room acoustics.

A series of tools are currently being developed around SyFaLa. While none of them has been officially released yet, you can follow their development/evolution on the project Git repository: https://gitlab.inria.fr/risset/syfala

URL: https://faust.grame.fr/syfala/

Contact: Tanguy Risset

7 New results

7.1 Flexible Radio Front-End

Activities in this axis could globally be divided in three main topics: wake-up radio and wireless power transfer, RFID systems and combination of spatial modulation and full-duplex, but also some other related topics.

7.1.1 Wake-Up radio and wireless power transfer

We have continued to work on wake-up radio systems but particularly increased our focus on Wireless Power Transfer (WPT). We proposed to model a full transmission chain with State-Space Models [4] in order to increase the overall efficiency of a WPT system by taking into account not only the optimization of the hardware parts, but also considering the radio channel characteristics. We also have started to study the potential of distributed beamforming at the sources level [3] to increase the total harvested energy by an ideal synchronization of distributed sources, this requiring a simple but efficient feedback mechanism.

7.1.2 RFID

On RFID systems, a work on Elastic yarns to directly integrate RFID antennas in textile for passive RFID systems was done, detailing the performance of an helix antenna using such a technology [1]. In parallel, we also worked on a theoretical evaluation of tag to tag communications to test the available communication quality that we can obtain depending on the distance, the placement and the position of the distant source in a scatter radio communication between two RFID tags [12].

7.1.3 Combination of spatial modulation and full-duplex

During the period, an important work was done to enhance the realism of the evaluation of combined Full-Duplex and Spatial Modulation architectures [6, 13, 14] to increase the spectral efficiency of radio links. A detailed study on the simulation of Spatial Modulation architectures was performed, taking into account the RF front-ends non-idealities to capture the behaviour of a realistic system.

7.1.4 Other related works

The bilateral collaboration with Radu Bozomitu, professor at the Technical University Gh Asachi Iasi, Romania, was initiated in 2018 during an Erasmus Mobility. Our research work focused on the implementation of an application for transmitting image notifications on the FM radio broadcasting infrastructure. This application is dedicated to warn drivers about significant road events and to increase the traffic safety and is based on the Software Defined Radio paradigm [2].

At a higher level, in the framework of the SPIE ICS chair we also published a high level survey on energy constraints for IoT devices to give some general trends and solutions to solve the problem of feeding billions of IoT devices [21].

7.2 Transiently powered systems and Non-Volatile Memory

Socrate is studying the new NVRAM (Non-Volatile Radom Access Memory) technology and its use in ultra-low power context. Many emerging technologies are forseen for Non-Volatile RAM to replace current RAM [28].

Socrate has started a work on the applicability of NVRAM for *transiently powered systems*, i.e. systems which may undergo power outage at any time. This study resulted in the Sytare software [24] and is also studied in an Inria Project Lab ZEP (`https://project.inria.fr/iplzep/teams/`).

7.2.1 The Sytare software: an operating system for transiently powered systems

In 2020 three important works were published, resulting on the research activities on Sytare. In LCTES conference [7] was proposed a formal proof of Sytare mecanism for restoring peripheral devices after power outage. In [9] was proposed a new promising checkpointing mechanism based on memory protection units (MPU) present in most modern microcontrolers. In [8] is proposed a high level way of predicting power consumption of sensor programs using peripherals. These three studies are described below.

In [8] we propose a methodology to measure, model and simulate power consumption of peripheral devices of a low-power embedded micro-controller, while keeping a reasonable development cost. This methodology is experimented against the low-power MSP-EXP430FR5739 platform that includes

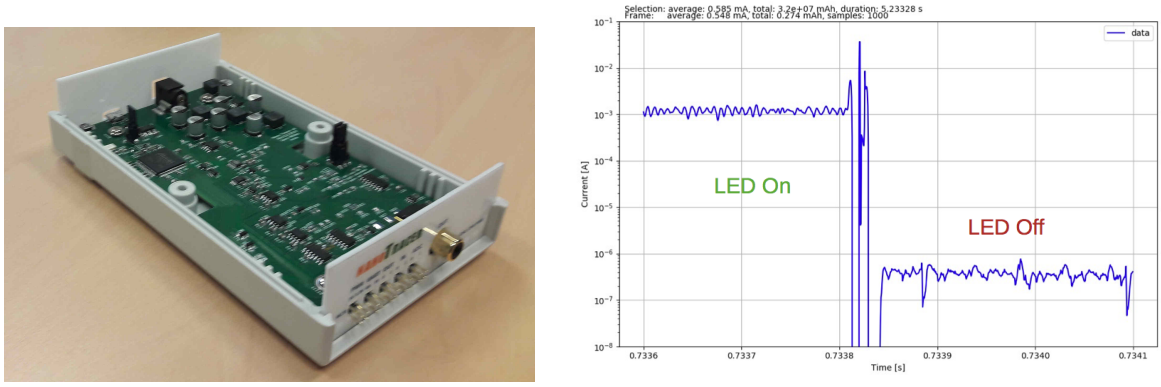

Figure 4: Photo (left) of first packaged nanoTracer prototype and snapshot (right) of a measurement provided by nanoTracer

nonvolatile RAM for intermittent computing purposes and a handful of peripherals. The experimental measurements enable the characterization of the consumption of the peripherals, while many existing comparable studies do not provide power consumption for peripherals. These measurements are integrated into a simulator that targets low-power peripheral-intensive applications, as are most of IoT embedded programs. The accuracy of the power consumption estimation is within a 5 percent error on intermittent embedded computing using peripherals.

In [9], we propose a new incremental checkpointing mechanism supported by a common hardware component, namely a Memory Protection Unit (MPU). This mechanism leverages the hardware interrupts of the MPU: volatile RAM is read-only on boot and is progressively unlocked as soon as protection violations occur. The MPU interrupt handler is designed to flag the corresponding volatile RAM blocks as dirty, i.e., modified. When a power outage is foreseen to be imminent, the software simply has to copy the dirty blocks from volatile RAM into the non-volatile RAM to ensure application progress over power outages. We validate our approach analytically and in cycle-accurate simulation, and we show that the proposed solution can be easily implemented on real hardware.

Finaly, after a long collaboration with formal proof researchers, Delphine Demange in Rennes and Pierre-Evariste Dagan in Paris, we were able to provide the first formal modeling of transiently powered systems, this was presented at LCTES [7] and submited to ACM TOPLAS journal. The initial motivation for this work was the following: as programmers, we are ill-equipped to reason about systems where power failures are the norm rather than the exception. A first challenge consists in being able to capture all the volatile state of the application – external peripherals included – to ensure progress. A second, more fundamental, challenge consists in specifying how power failures may interact with peripheral operations. In [7], we propose a formal specification of intermittent computing with peripherals, an axiomatic model of interrupt-based checkpointing as well as its proof of correctness, machine-checked in the Coq proof assistant. We also illustrate our model with several systems proposed in the literature.

7.2.2 A high-performance ammeter for embedded systems

By the end of 2019, the socrate team designed and built a high performance ammeter dedicated to power measurements for small devices. Our prototype measures currents between 100nA and 100mA (gain is audo-adjusted dynamically) with a sampling frequency of 2Msps. Data is streamed to a PC over USB which enables long-running experiments, or just real-time visualization of data, see Fig. 4.

In 2020, Gero Müller who had started this work left Inria but continued to maintain the private `git` project of nanotracer (`https://geromueller.de/nanotracer/`). Because of Covid pandemy, the test conducted at Inria (Alexandre Abadie from the IoT SED team) has been delayed, but we are still convinced that this material can be useful to many engineers.

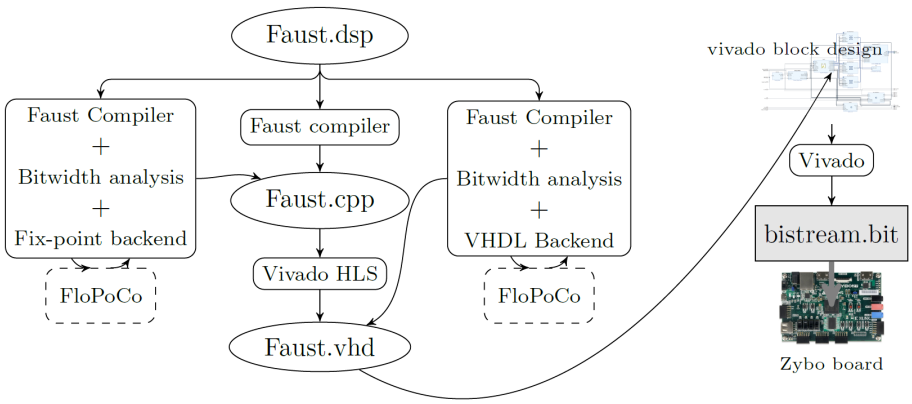

Figure 5: The complete faust2FPGA studied in future FAST ANR project. The central flow has been prototyped and presented in [16].

7.2.3 Ultra-low latency audio on FPGA

Part of the Socrate team is involved in the creation of a new Inria project focussed on Embedded Programmable Audio Systems (Emeraude team proposal) in association with the the researchers of the GRAME group (https://www.grame.fr/recherche). GRAME is a "Centre National de Création Musicale" (CNCM) organized in three departments: music production, transmission/mediation, and computer music research. Four GRAME researchers have expertise in computer science (compilation), audio DSP, digital lutherie, and human-computer interaction in general. GRAME has been leading the development of the FAUST [2] programming language since its creation in 2004.

Socrate and GRAME have started a collaboration through the Syfala *(synthèse audio faible latence)* project (https://faust.grame.fr/syfala/) whose goal is to design an FPGA-based platform for multichannel ultra-low-latency audio Digital Signal Processing (DSP), programmable at high-level with FAUST and using Socrate's software FloPoCo (http://flopoco.gforge.inria.fr). A first very preliminary version of this compiler was presented at IFC2020 [16] (see Fig. 5), an earlier presentation was made at PAW workshop 2019 (Programmable Audio Workshop: https://paw.grame.fr/). In septembre 2020 an ANR project (FAST: Fast Audio Signal-processing Technologies on FPGA) was accepted on this topic.

7.3 Computer arithmetic

Florent de Dinechin has worked on a book, *Application-Specific Arithmetic* co-authored with Martin Kumm (Hochschule Fulda Germany) to be published by Springer in 2021. He has been invited to a special session of the DATE conference (Design And Test in Europe) about *Next Generation Arithmetic for Edge Computing* [10].

7.3.1 Embedding arithmetic optimizations in compilers

In [5], Socrate studies hardware-specific optimization opportunities currently unexploited by HLS compilers. Some of these optimizations are specializations of floating-point operations. They respect the usual semantics of the input program while other optimizations do not, assuming instead that a floating-point computation is actually intended to compute with real numbers. What matters then is to respect application-level accuracy constraints, expressed as pragmas in the source code. This provides the compiler with freedom to use non-standard arithmetic when more efficient. A source-to-source compiler is used to prototype the proposed optimizations and evaluate them on relevant benchmarks.

[2] FAUST is a domain specific language for real-time audio signal processing primarily developed at GRAME-CNCM and by a worldwide community. FAUST is based on a compiler "translating" DSP specifications written in FAUST into a wide range of lower-level languages (e.g., C, C++, Rust, Java, WASM, LLVM bitcode, etc.). Thanks to its "architecture" system, generated DSP objects can be embedded into template programs (wrappers) used to turn a FAUST program into a specific ready-to-use object (e.g., standalone, plug-in, smartphone app, webpage, etc.).

7.3.2 A general technique for lossless table compression

Hsiao et al. recently introduced, in the context of multipartite table methods, a lossless compression technique that replaces a table of numerical values with two smaller tables and one addition. Work in Socrate [19] has improved this technique and the resulting architecture by exposing a wider implementation space, and an exhaustive but fast algorithm exploring this space. It also shows that this technique has many more applications than originally published, and that in many of these applications the addition is for free in practice. These contributions are implemented in the open-source FloPoCo core generator, where some tables can be compressed by a factor 2.

7.4 Environmental Impact

Because of the evolution of the socrate team mentionned in section 3.3, Socrate member are increasingly involved in topic related to numerical ecological transition. Kevin Marquet took the co-direction of GDS EcoInfo (CNRS) since September 2019: http://ecoinfo.cnrs.fr. He is also collaborating with the Inria Spades team, first by co-supervising a PhD student on the environmental issues of digital technology, then by participating in reading workshops, once a month, on related themes. He is also participating in the creation of an Inria Challenge on digital sobriety, coordinated by Sophie Quinton and Peter Sturm.

Training in environmental issues is of growing importance. In this context, we have, with several colleagues, developed a knowledge repository intended to help teachers to set up courses on this subject [18].

Kevin Marquet and Guillaume Salagnac are involved in the creation of a team called Phenix focussed on Frugal IT and emancipatory security for a digital transition.

8 Bilateral contracts and grants with industry

8.1 Bilateral contracts with industry

Research Contract with Bosch 2020 In collaboration with Aric, Socrate worked with Bosch on the implementation of the square root function the context of an embedded processor.

Research Contract with SafeHear 2020 Socrate worked with recent start-up SafeHear http://safehear.fr on a an advanced professional headset, the collaboration mainly consisted in an internship advisoring.

9 Partnerships and cooperations

9.1 European initiatives

9.1.1 Collaborations in European programs, except FP7 and H2020

New European CIG Project: IMMUNet is a European CIG project (Cost Innovators Grant) lead by University of Bologna (Italy), studying high TRL solution for Industrial Machine Monitoring with wireless sensors using LoRa physical layer and Energy harvesting.

9.2 National initiatives

Insa-Spie IoT Chair The Insa-Spie IoT Chair http://www.citi-lab.fr/chairs/iot-chair/ relies on the expertise of the CITI Lab. The skills developed within the different teams of the lab integrate the study, modelling, conception and evaluation of technologies for communicating objects and dedicated network architectures. It deals with network, telecom and software matters as well as societal issues such as privacy. The chair will also lean on the skills developed at INSA Lyon or in IMU LabEx. in the framework of this chair we published a survey paper on energy consumption of IoT devices [21].

Inria Project Lab: ZEP The ZEP project addresses the issue of designing tiny computing objects with no battery by combining non-volatile memory (NVRAM), energy harvesting, micro-architecture innovations, compiler optimizations, and static analysis. The main application target is Internet of Things (IoT) where small communicating objects will be composed of this computing part associated to a low-power wake-up radio system. The ZEP project gathers four INRIA teams that have a scientific background in architecture, compilation, operating system and low power together with the CEA Lialp and Lisan laboratories of CEA LETI & LIST.

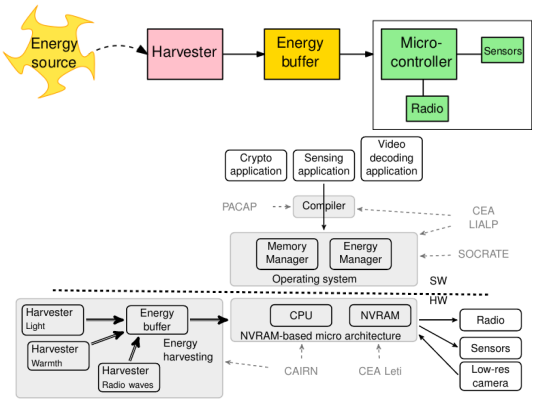

Figure 6: Example of system targeted by the ZEP project on the left, and on the right: the ZEP research program.

The scientific work (in progress) is organized around three fields :

- specific NVRAM-based architecture
- dedicated compiler pass that computes a worst-case energy consumption
- operating system managing NVRAM and energy, ensuring memory consistency across power outages

The project is illustrated by the figure 6, where PACAP, SOCRATE, CORSE, and CAIRN are the teams involved in the project.

ANR - Imprenum The objective of this project (INSA-Lyon, École Normale Supérieure de Lyon, CEA LETI) is to promote **accuracy as a first class concern** in all the levels of a computing system:

- at the hardware level, with better support for lower-than-standard and higher-than-standard precisions;
- at the level of run-time support software, in particular answering the memory management challenges entailed by adaptive precision;
- at the lower level of mathematical libraries (kernel level), for instance BLAS for linear algebra, enhancing well established libraries with precision and accuracy control;
- at the higher level of mathematical libraries (solver level, including algebraic linear solvers such as LAPACK, ad hoc steppers for Ordinary Differential Equation, eigenvalues kernels, triangularization problems for computational geometry, etc.) Here, accuracy and precision control of the lower levels should enable higher-level properties such as convergence and stability;
- at the compiler level, enhancing optimising compilers with novel optimisations related to precision and accuracy;
- at the language level, embedding accuracy specification and control in existing languages, and possibly defining domain-specific languages with accuracy-aware semantics for some classes of applications.

ADT SytaRiot The objective of this ADT was initially to make Riot (https://www.riot-os.org/) compatible with NVRAM-based architecture, therefore to integrate Sytare with Riot (https://gitlab.inria.fr/citi-lab/sytare/) and thus open Riot to ultra low power platforms containing NVRAM, *eg* Texas microcontrollers Instrument MSP430FR5969.

After having completed this task, the hired engineer left and we re-orient the ADT toward the new project studied by Socrate (towards the creation of the Emeraude project): ultra low latency audio on FPGA.

Digital Hardware AI Architectures Florent de Dinechin participates to the chair *Digital Hardware AI Architectures* held by Prof. Frédéric Pétrot at the Multidisciplinary Institute in Artificial Intelligence (MIAI) of Grenoble. The other participants are François Duhem (Spintec/CEA) and Fabrice Rastello (LIG/Inria), with industrial partners Google France, Kalray, STMicroelectronics, and Upmem.

This chair funds the PhD of Maxime Christ, which studies how very low-precision arithmetic formats may improve the efficiency of the learning phase of neural networks.

10 Dissemination

Member of Conference Program Committees Tanguy Risset was a member of the program committee for DATE 2021 (Design Automation and Test in Europe), on track " Architectural and Microarchitectural Design".

Florent de Dinechin was a member of the program committee for ARITH (International Symposium on Computer Arithmetic), COMPASS (Conférence francophone d'informatique en Parallélisme, Architecture et Système), FCCM (FPGA-based custom-computing machines), and FPT (Field-Programmable Technologies).

Invited talks Florent de Dinechin gave an invited talk entitled *Hardware and FPGAs computing just right* at the workshop *Variable Precision in Mathematical and Scientific Computing* organized in May 2020 by ICERM (the Institute for Computational and Experimental Reserch in Mathematics.

Research administration

- Tanguy Risset was deputy director of the FIL (Fédération Informatique de Lyon) until dec. 2020.
- Florent de Dinechin was head of Citi Lab until end dec. 2020.

10.1 Teaching - Supervision - Juries

10.1.1 Teaching

- Tanguy Risset is professor at the Telecommunications Department of Insa Lyon.
- Florent de Dinechin is a professor at the Computer Science Department of Insa Lyon. He also teaches computer architecture at ENS-Lyon.
- Guillaume Salagnac and Kevin Marquet are associate professors at the Computer Science Department of Insa Lyon.
- Guillaume Villemaud and Florin Hutu are associate professor at the Electrical Engineering Department of Insa Lyon.

10.1.2 Supervision

- PhD in progress : **Gautier Berthou** : *Operating system for transiently powered systems*, Inria, (IPL ZEP) since 01/2018.
- PhD in progress : **Luc Forget** : *Algèbre linéaire calculant au plus juste*, ANR Imprenum, since 10/2018.

- PhD in progress :**Yanni Zhou** : *Full Duplex and spatial modulation* since 10/2018
- PhD in progress : **Tarik Lassouaoui** : *Tag 2 Tag communication* since 10/2018
- PhD in progress : **Regis Rousseau** : *Wireless Power Transfer* since 10/2018
- PhD starting : **Maxime Christ** : *Learning in Very Low Precision* since 10/2018
- PhD defended : **Andrea Bocco**: *A variable precision hardware acceleration for scientific computing*, École Doctorale MathInfo, 29/07/2020.

10.1.3 Juries

- Tanguy Risset was a member of the jury of the following theses:
  - Florian Arrestier (reviewer, INSA Rennes)
  - Guillaume Patrigeon (jury U. Montpelier)
- Florent de Dinechin was a member of the jury for
  - Andrea Bocco (INSA-Lyon)
  - Niloofar Charmchi (U. Rennes 1)

11 Scientific production

11.1 Publications of the year

International journals

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[5] Y. Uguen, F. De Dinechin, V. Lezaud and S. Derrien. 'Application-specific arithmetic in high-level synthesis tools'. In: *ACM Transactions on Architecture and Code Optimization* (1st Mar. 2020). DOI: 10.1145/3377403. URL: https://hal.archives-ouvertes.fr/hal-02423363.

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International peer-reviewed conferences

[7] G. Berthou, P.-E. Dagand, D. Demange, R. Oudin and T. Risset. 'Intermittent Computing with Peripherals, Formally Verified'. In: *LCTES '20: 21st ACM SIGPLAN/SIGBED Conference on Languages, Compilers, and Tools for Embedded Systems Proceedings*. LCTES '20 - 21st ACM SIGPLAN/SIGBED Conference on Languages, Compilers, and Tools for Embedded Systems. London / Virtual, United Kingdom, June 2020, pp. 85–96. DOI: 10.1145/3372799.3394365. URL: https://hal.inria.fr/hal-02556878.

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[10] A. Guntoro, C. De La Parra, F. Merchant, F. De Dinechin, J. Gustafson, M. Langhammer, R. Leupers and S. Nambiar. 'Next Generation Arithmetic for Edge Computing'. In: DATE 2020 - Design, Automation and Test in Europe Conference. Grenoble, France, 9th Mar. 2020, pp. 1357–1365. DOI: 10.23919/DATE48585.2020.9116196. URL: https://hal.inria.fr/hal-03114381.

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[16] T. Risset, R. Michon, Y. Orlarey, S. Letz, G. Müller and A. Gbadamosi. 'Faust2FPGA for Ultra-Low Audio Latency: Preliminary work in the Syfala project'. In: IFC2020 - Internationnal Faust Conference. paris, France, 1st Dec. 2020. URL: https://hal.inria.fr/hal-03116958.

Doctoral dissertations and habilitation theses

[17] A. Bocco. 'A variable precision hardware acceleration for scientific computing'. Université de Lyon, 29th July 2020. URL: https://tel.archives-ouvertes.fr/tel-03102749.

Reports & preprints

[18] P. Boulet, S. Bouveret, A. Bugeau, E. Frenoux, J. Lefevre, A.-L. Ligozat, K. Marquet, P. Marquet, O. Michel and O. Ridoux. *Référentiel de connaissances pour un numérique éco-responsable*. EcoInfo, 30th Sept. 2020. URL: https://hal.archives-ouvertes.fr/hal-02954188.

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